(12) PATENT APPLICATION PUBLICATION
(19) INDIA
(22) Date of filing of Application :27/06/2021

(21) Application No.202141028829 A
(43) Publication Date : 09/07/2021

(54) Title of the invention : TRANSMISSION GATE VOLTAGE LEVEL TRANSLATOR FOR DEEP SUB-MICRON TECHNOLOGY

(51) International classification	:H03K0003356000, H03K0019018500, H03K0017687000, H03K0003030000, H03K0019000000
(31) Priority Document No	:NA
(32) Priority Date	:NA
(33) Name of priority country	:NA
(86) International Application No Filing Date	:NA :NA
(87) International Publication No	: NA
(61) Patent of Addition to Application Number Filing Date	:NA :NA
(62) Divisional to Application Number Filing Date	:NA :NA

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(57) Abstract :
A Transmission Gate Voltage level translator for deep sub-micron technology is a digital circuit does voltage level translating. The circuit includes a short circuit aware inverter and a transmission gate based voltage level translation and signal blocking; wherein the digital circuit comprises 2 X 1 Multiplexer to select VDDH or VDDL with one NMOS transistor and one PMOS transistor in the level shifting selection stage; wherein the digital circuit receives an input voltage (VIN) from the multi voltage supply circuits and produces an output voltage (VOUT) when the BLOCK input is given ˜0™; wherein the input VIN has a voltage swing between VDDL and VDDH supply voltages; wherein the output VOUT has a voltage swing between VDDH and VDDL supply voltages; and wherein the level translator circuit selects type of level translation in response to a level of the input voltage. When the BLOCK input is given ˜1™ the signal is completely blocked. The short circuit aware Inverters and Transmission gates as switching elements provides low power consumption and Delay even at higher frequencies.

No. of Pages : 17 No. of Claims : 5