

ACADEMIC REGULATIONS
COURSE STRUCTURE
AND
DETAILED SYLLABUS (As per AICTE Model Curriculum)
for

M. Tech Two Year Degree Course

2019-2020

Digital Systems and Computer Electronics
(ECE)



A U T O N O M O U S
SREENIDHI INSTITUTE OF SCIENCE & TECHNOLOGY
(An Autonomous Institution approved by UGC and affiliated to JNTUH)
Yammampet, Ghatkesar Mandal, Hyderabad - 501 301.

ACADEMIC REGULATIONS FOR M. Tech (Full-Time) PROGRAMS - 2019-20 (A-19)

(Effective for the students admitted into first year from the academic year 2019-20 and onwards)

1.0 Post-Graduate Degree Programmes in Engineering & Technology (PGP in E&T) offered BY Sreenidhi Institute of Science And Technology is a **Two Year (Four Semesters)** full-time Master of Technology (M.Tech.) Post Graduate Programmes, under Choice Based Credit System (CBCS) and is affiliated to JNTUH.

2.0 ELIGIBILITY FOR ADMISSIONS:

2.1 Admission to the PGPs shall be made subject to eligibility, qualification and specializations prescribed by the University and as adopted by Sreenidhi Institute of Science and Technology from time to time, for each specialization under each M.Tech program.

2.2 Admission to the post graduate program shall be made on the basis of either the merit rank or Percentile obtained by the qualified student in the relevant qualifying GATE Examination / the merit rank obtained by the qualified student in an entrance test conducted by Telangana State Government (PGECET) for M.Tech programs, or on any other exams approved by the University, subject to reservations as laid down by the Government from time to time.

2.3 The medium of instruction for all PG Programs will be **ENGLISH** only.

3.0 M.Tech Programs Structure:

3.1 The M.Tech Programs are of Semester pattern, with **Four Semesters** consisting of **Two** academic years, each academic year having **Two Semesters** (First/Odd and Second/Even Semesters). Each Semester shall be of 22 weeks duration (inclusive of Examinations), with a minimum of 90 instructional days per Semester.

3.2 **The student shall not take more than four academic years to fulfill all the academic requirements for the award of M.Tech degree from the date of commencement of first year first semester, failing which the student shall forfeit the seat in M.Tech program.**

3.3 **UGC/AICTE** specified definitions / descriptions are adopted appropriately for various terms and abbreviations used in this PG academic regulations.

3.3.1 Semester Scheme:

Each Semester shall have 'Continuous Internal Evaluation (CIE)' and 'Semester End Examination (SEE)'. Choice Based Credit System (CBCS) and Credit Based Semester System (CBSS) are taken as 'references' for the present set of Regulations. The terms 'SUBJECT' imply the same meaning here and refer to 'Theory Subject', or 'Lab Course', or 'Seminar', or 'Comprehensive Viva', "Project" or 'Technical Paper Writing' as the case may be.

3.3.2 Credit Courses:

All students in a semester to earn credits which shall be assigned to each subject / course in an L: T: P: C (Lecture Periods: Tutorial Periods: Practical Periods: Credits) structure based on the following general pattern:

3.3.2.1 One credit for every one hour of theoretical lectures undergone per week during the entire semester. In case of tutorials one credit for every one hour of tutorials undergone per week during the entire semester. One credit for every two hours of laboratory practical, technical seminar, Comprehensive Viva Voce, Mini Project with seminar, Project phase – I with seminar, Project phase – II with seminar, for the instruction undergone per week during the entire semester.

3.3.2.2 Other student activities like guest lecture, conference / workshop participations, and technical paper presentations are not given any credits. However, if they produce evidence that they have attended such programs, attendance will be given for the respective subject periods shown as per the time table which are lost due to their participation elsewhere. For the mandatory courses, they have to put in attendance which will be added to the attendance to the other subjects and decide whether a student can be permitted to write the examinations or not. There will be no credits given for the mandatory and audit courses but their performance will be judged and

graded as follows

Percentage of marks secured in a Audit course	Grade
Greater than or equal to 90%	Outstanding
80% and above but less than 90%	Excellent
70% and above but less than 80%	Very good
60% and above but less than 70%	Good
50% and above but less than 60%	Above Average
Less than 50%	Fail
Absent	Ab

3.3.3 **Additional Credits:**

In case of M.Tech programs, a student can register a minimum of 17 credits and maximum of 24 credits to complete theory courses to concentrate on Project work in the II year. However, he / she will be given provisional certificate only at the end of two years even if he / she has completed all the requirements before that. **The candidate has to complete the course within four academic years from the date of his / her admission.**

3.3.4 **Subject Course Classification:**

All subjects / courses offered for the Post-Graduate Programs of M. Tech are classified as follows. The Institution has followed the general guidelines issued by AICTE.

S.No.	Broad Course Classification	Course Group/ Category	Course Description
1	Core Courses (CoC)	PC - Professional Core	Includes subjects related to the parent Discipline / Department / Branch.
		Project Work	M.Tech Project or Mini - Project or Major-Project or as applicable.
		Seminar, Technical seminar	Seminar on core contents related to parent discipline / department / branch.
		Comprehensive Viva-Voce	Viva-voce covering all the PG subjects studied during the course work.
2	Elective Courses (Ele)	PE - Professional Electives	Includes elective subjects related to the parent discipline / department / branch
		OE - Open Electives	Elective subjects which include inter- disciplinary subjects or subjects in an area outside the parent discipline / department / branch.
3.	Audit course	AC - Audit courses	1. English for Research paper writing (Grade evaluation). 2.Ethics, Morals, Gender sensitization and Yoga (Grade evaluation)
Total number of Credits – 68 for M.Tech			

4. **M.TECH COURSES**

Departments offering M.Tech. Programmes with specializations are noted below:

Sl. No.	Department	M.Tech Course
1	CSE	Computer Science
2	CSE	Computer Science and Engineering
3	EEE	Electrical Power Engineering
4	ECE	Digital Systems and Computer Electronics

5	ME	CAD / CAM
6	ME	Thermal Engineering
7	IT	Computer Networks and Information Security

5.0 Attendance Requirements:

- 5.1 A student shall be eligible to appear for the semester end examinations, if student acquires a minimum of 75% attendance in aggregate of all the subjects / lab subjects / seminars / Mini and major projects (excluding attendance in mandatory / audit courses, NCC / NSO and NSS) for that semester.
- 5.2 Shortage of attendance in aggregate up to 10% (65% and above, and below 75%) in each semester may be condoned by the College Academic Committee on genuine and valid grounds, based on the student's representation with supporting evidence.
- 5.3 A stipulated fee shall be payable towards condoning of shortage of attendance.
- 5.4 Shortage of attendance below 65% in aggregate shall in **NO CASE** be condoned.
- 5.5 Students whose shortage of attendance is not condoned in any semester are not eligible to take their end examinations of that semester. They get detained and their admission for that semester shall stand cancelled. They shall not be promoted to the next semester. They may seek re-admission in that semester in which student was detained as and when offered. In case, if there are any professional electives and / or open electives, the same may also be opted, if offered. However, if those electives are not offered in later semesters, then alternate electives may be chosen from the same set of elective subjects offered under that category.
- 5.6 A student fulfilling the attendance requirement in the present semester shall not be eligible for readmission into the same semester.

6.0 Academic Requirements:

- The following academic requirements have to be satisfied, in addition to the attendance requirements mentioned in item no. 5. The performance of the candidate in each semester shall be evaluated subject-wise, with a maximum of 100 marks per subject (theory / practical), on the basis of Continuous Internal Evaluation and Semester End Examination.
- 6.1 A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject, if he / she secures not less than 40% of marks (30 out of 75 marks) in the End Semester Examination, and a minimum of 50% of marks in the sum total of CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together; in terms of Letter Grades and this implies securing "B" Grade or above in a subject.
- 6.2 A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to a subject, if he / she secures not less than 50% of the total marks. The student is deemed to have failed, if he / she (i) does not attend the comprehensive viva-voce as per the schedule given, or (ii) does not present the seminar as required, or (iii) does not present the Technical seminar as required. In such a case, he / she may reappear for comprehensive viva-voce in supplementary examinations and for seminar / technical paper writing, in the subsequent semesters, as and when scheduled by paying required fee as per the norms of the Institution.
- 6.3 A student shall register for all subjects with the total credits of 68 for M.Tech courses as specified and listed in the course structure for the chosen specialization, and has to put in required attendance and fulfill all the academic requirements of securing a minimum of 'B' Grade or above in each subject, and securing Semester Grade Point Average (SGPA) of 6.0 (in each semester) and final Cumulative Grade Point Average (CGPA) (i.e., CGPA at the end of PGP) of 6.0, to complete the PGP successfully.

Note: (1) The SGPA will be computed and printed on the marks memo only if the candidate passes in all the subjects offered and gets minimum B grade in all the subjects.

- (2) CGPA is calculated only when the candidate passes in all the subjects offered in all the semesters.**

- (3) **The Institution will give grade card / marks memo at the end of each semester. In any semester in which a mandatory / audit course is offered the results of these subjects will be given in the letter grade as mentioned in item 10.2 given in latter sections of these regulations in the grade cards / marks memo of the corresponding semester.**
- 6.4 Marks and Letter Grades obtained in all those subjects covering the above specified credits alone shall be considered for the calculation of final GPA, which will be indicated in the Grade Card /Marks Memo of second year second semester. In addition, the letter grades secured by the students in the mandatory / audit subjects will also be mentioned in the grade card / marks memo of II year II semester.
- 6.5 If a M.Tech student registers for extra subject(s) (in the parent department or other departments / branch) other than those listed subjects totaling to 68 credits respectively as specified in the course structure, the performance in extra subject(s) (although evaluated and graded using the same procedure as that of the required 68 credits) will not be taken into account while calculating the SGPA and CGPA. The extra subject(s) shall be from open elective / professional elective. Additional fee has to be paid for registering for extra subjects which are not required with regard to the credit requirements. For such extra subject(s) registered, percentage of marks and Letter Grade alone will be indicated in the Grade Card / Marks Memo, as a performance measure, subject to satisfying the attendance and academic requirements as stated in items 5 and 6.1 - 6.3.
- 6.6 When a student is detained due to shortage of attendance in any semester, no Grade allotment will be made. However, the student is eligible for re-admission in the subsequent semester(s), as and when next offered, with the academic regulations of the batch into which the student is re-admitted, by paying the prescribed fee as per the norms of Institution. In all these re-admitted cases, the student shall have to secure a fresh set of internal marks and Semester End Examination marks for performance evaluation and SGPA / CGPA calculations.
- 6.7 A student eligible to appear for the Semester End Examination in any subject, but absent from it or failed (failing to secure 'B' Grade or above), may reappear for that subject at the supplementary examination as and when conducted. In such cases, his Internal Marks assessed earlier for that subject will be carried over, and added to the marks secured in the supplementary examination, for the purpose of evaluating his performance in that subject(s).
- 6.8 A student can opt for one extra subject from II year I semester in M. Tech. I year I semester and also in I year II semester so that the student can complete all the subjects of II year I semester in advance and student can concentrate on Project work in the entire II year either in the institution or in the industry to complete quality work.
- 6.9 **A Student who fails to earn 68 credits in M.Tech program as per the specified course structure, and as indicated above, within four academic years from the date of commencement of his / her first year first semester, shall forfeit his / her seat in M.Tech program and his / her admission shall stand cancelled.**
- 7.0 **EVALUATION:**

The performance of a student in each semester shall be evaluated subject- wise (irrespective of credits assigned) for a maximum of 100 marks. The M.Tech project work (major project) will also be evaluated for 100 (30 CIE and 70 SEE) marks.

7.1 Each subject / Lab will have total of 100 marks (30 CIE and 70 SEE). There shall be two midterm examinations in every theory subject. 23 marks are earmarked for each midterm examination. **The marks shall be awarded considering the average of two midterm examination marks in each subject.** If any candidate is absent or if he wishes to improve the sessional marks he can appear for third mid-term examination. The syllabus for the third Mid examination shall be the entire syllabus of the subject concerned, and conducted on the same day of main examination. **The result of third mid test will be treated equal to that of a mid test and average of the better two out of the three mid tests will be considered.**

Each mid test will have compulsory questions without choice and long answer questions as detailed in the following paragraphs.

- Separate registration for the third mid examination has to be done by the student for each of the subjects the student wishes to appear for. He has to pay an examination fee as prescribed by the college per subject from time to time.
- **The midterm examination** question paper shall be of three parts, i.e. Part ‘A’, Part ‘B’ and Part ‘C’.

The following procedure is to be followed for internal evaluation as given in the below table

Item	Proposed Marks
a) Part – A of Mid Test	12 questions – Short type questions 6 marks
b) Part – B of Mid Test will have 3 questions (1 from each unit) and student has to answer 2 questions	2 Questions out of 3 questions 14 marks
c) Part – C Mid test	Question Paper will have 3 questions, one question from each unit will be chosen out of 3 questions given for assignment. Student has to answer any one question out of 3 questions. 3 marks
d) Assignment	For assignment -1, three questions from each unit- total of 9 questions to be submitted before first mid test. Similarly assignment – II will be given to be submitted before II Mid test and average of two assignments will be considered. 2 marks
e) Class room participation and attendance	3 marks
f) Class notes	2 marks
Total Marks	30 Marks

- Mid Exam – I – First three Units - Duration – 2 hours
- Mid Exam – II – Last three Units - Duration – 2 hours
- Mid Exam – III – All six units - Duration – 2 ½ hours
- Two assignments shall be given for a total weightage of 2 marks.

- Assignment - I for 2 Marks is to be submitted at least one week before the first mid examinations.
- Second assignment also will carry 2 marks for the remaining 3 units which is to be submitted at least one week before the second mid examination.
- The average of the two assignments will be taken with a total weightage of 2 marks.
- Students will have to be give back the assignment before each mid examination.
- Besides this 2 marks are allotted for class notes which is to be signed by concerned teacher for every fortnight.

Three marks for each theory subject shall be given for the students based on class room participation and attendance which they have put in a graded manner as per the table given below:

S.No.	Attendance Range	Marks Awarded
1.	65 % and above but less than 75%	1
2.	75% and above but less than 85%	2
3	More than 85 %	3

- **Calculation of final sessional marks for each subject:**

Sl.No	The item of evaluation of sessional marks	Maximum marks	Total marks scored in the subject by the student
1	Mid sessional examinations	23	
2	Assignments	2	
3	Class room participation & Attendance	3	
4	Class notes	2	
Total marks		30 marks	

7.1.1 The external examination question paper shall be of two parts, Part 'A' and Part 'B'.

Pattern for External Examinations (70 marks):

1. For Theory Subjects

There shall be external examination in every theory subject and it consists of two parts (Part-A & Part-B). The total time duration will be 3 hours.

- Part - A will be of 20 marks, which will have 10 short questions, which is compulsory.

- Part-B will be of 50 marks, which will have subjective type questions and shall have 7 questions out of which 5 are to be answered. At least one question must appear from each unit such that not more than 2 questions from any unit. All the questions carry equal marks.

Pattern of Evaluation for Lab Subjects (100 marks):

It is decided to offer one lab subject in I semester and one lab subject in the II semester of I year for M.Tech courses. For practical subjects there shall be a continuous evaluation during the semester for 30 sessional marks and 70 marks for end examination.

Assessment of internal marks (30 marks) will be as follows:

1. Day-to-Day work	- 05 marks
2. Final Record and viva	- 05 marks
3. Average of two tests including viva	- 10 marks
4. Lab based project report and viva	- 05 marks
5. Lab Project demo	- 05 marks
Total	- 30 marks

Pattern of end examinations:

The end examination in each lab subject will be for 70 marks. The conduct of the end examination shall be the team consisting of an external examiner and an internal examiner appointed by the Chief Superintendent of Examinations of the college. The marks are distributed as follows:

Procedure of experiment and calculation	- 10 marks
1. Conduct of experiment, observation, calculation	- 20 marks
2. Results including graphs, discussions and conclusion - 20 marks	
3. Viva voce and record	- 20 marks
Total	- 70 marks

In case of computer lab subjects the assessment will be as follows:

Assessment of sessional marks (30):

1. Flowchart and algorithms	- 05 marks
2. Program writing and execution	- 15 marks
3. Result and conclusions	- 05 marks
4. Viva voce and record	- 05 marks
Total	- 30 marks

Assessment in the end semester examination (70 marks):

1. Program description	- 10 marks
2. Program writing	- 15 marks
3. Program Execution	- 10 marks
4. Results and Conclusion	- 20 marks
5. Viva Voce	- 10 marks
6. Record and Observation	- 05 marks
Total	- 70 marks

For practical subjects there will be no recounting or re-valuation.

- 7.2 Each faculty member in-charge of the lab subject concerned must draw the normal distribution curve and submit to the HoD who in turn shall present the sessional marks analysis to the college academic committee. After discussion on the matter a decision will be taken by CAC whether to forward the entire material available with the teacher concerned for verification of the sessional marks awarded. A decision will be taken by the committee whether to moderate the marks awarded or not. The marks awarded by the committee shall be final and binding.
- 7.3 A candidate shall be deemed to have secured the minimum academic requirement in a theory subject / practical subject / other subjects if any which have both internal assessment and external assessment components, if he secures a minimum of 40% of marks in the End Examination and a minimum aggregate of 50% of the total marks allotted for that subject (internal marks and end semester exam marks put together). In case there is only internal assessment for a subject the marks secured in the sessional marks shall have to be at least 50%.
- 7.4 In case the candidate does not secure the minimum academic requirement in any subject in theory or practicals or others if any (as specified in 7.3) he/she has to reappear for the supplementary examination in that subject.

7.5. Distribution of marks for Seminars and Comprehensive Viva:

7.5.1 Technical seminar for M.Tech courses :

Technical seminar is divided into four parts one in each semester as stated below:

Semester	Subject	Credits	Internal marks	External marks
I year I semester	Technical seminar - I	1	100	-
I year II semester	Technical seminar – II	1	100	-
I year II semester	Mini project with seminar (Carried out in I year II semester and evaluated in II year I semester)	3	30	70
I year II semester	Comprehensive Viva Voce	1	30	70
II year I semester	Project Phase – I and Seminar	5	30	70
II year II Semester	Project Phase – II and Seminar	6	30	70
II year II Semester	Dissertation and defense viva	7	30	70

There shall be technical seminar during I year I semester and I year II semester, comprehensive viva voce in I year II semester and Mini Project with seminar during I year II Semester. For technical seminar, a student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the Department in a report form and shall make an oral presentation before the Departmental Committee, which shall consist of the Head of the Department, a senior Faculty Member and the Supervisor and will jointly evaluate the report and presentation. For each Seminar there will be only internal evaluation of 100 marks. A candidate has to secure a minimum of 50% to be declared successful. The comprehensive Viva voce in the subjects of I year I semester and I year II semester put together will be conducted by the External examiner and it will be for 70 marks and internal evaluation will be for 30 marks (total 100 marks), will be conducted at the end of 1st year 2nd semester. A candidate has to secure a minimum of 50% to be declared successful.

In the First semester seminar report must be in the form of the review paper with a format used by IEEE / ASME etc. In the Second semester Mini project with seminar in the form of Independent Review Paper must be of high quality fit for publication in a reputed conference / journal.

The evaluation format for seminar is as follows:

Selection of topic, literature survey Review by the guide	10 marks
Final report and viva	10 marks
Level of content	15 marks
Presentation	20 marks
Discussion & Involvement	15 marks
Class notes	15 marks
Attendance	15 marks
Total	100 Marks

7.6 Comprehensive Viva-Voce:

There shall be a Comprehensive Viva-Voce Examination at the end of I year II semester. The Comprehensive Viva-Voce will be conducted by a Committee consisting of Head of the Department and one Senior Faculty member of the Department and external examiner. The Comprehensive Viva-Voce is aimed to assess the student's understanding in various subjects, he / she studied during the M.Tech I year I semester and I year II semester. The Comprehensive viva voce is valued for 100 marks. There are 30 internal marks. For awarding these marks internal viva-voce test must be conducted twice in the semester – one at the end of 7 weeks and the other one at the end of 14 weeks. The average of two internals will be considered for 30 marks. 70 marks are to be awarded for external examination for comprehensive viva voce and he / she has to secure 40% of the marks to be successful in the external. A candidate has to secure a minimum of 50 % of marks in the sum total of internal and external to be declared successful.

S. No.	Description	Marks
1	Average of First & Second Mid Sessional Viva (Internal)	30

2	Final Viva during practical examinations (External)	70
	Total	100

7.7 Project Seminars:

In II year I semester and II semester there will be Project Phase – I with seminar, Project Phase – II with seminar. It shall be conducted for 30 marks internal and 70 marks external. A candidate has to secure a minimum of 40% of marks in the external examination. The Internal evaluation for the project shall be done in 2 stages (not less than 4 weeks between two consecutive stages). A candidate shall secure a minimum 50% of marks in sum total of internal and external to be declared successful.

Project work Phase I and II:

The student shall submit a project status report at the end of II year I semester along with a review paper on the subject of the thesis and same shall be evaluated at the end of the semester by the Project Review Committee (PRC).

8.0 EVALUATION OF PROJECT / DISSERTATION WORK:

Every candidate shall be required to submit a thesis or dissertation on a topic approved by the Project Review Committee.

- 8.1 A Project Review Committee (PRC) shall be constituted with Head of the Department as Chairperson, Project Supervisor and one senior faculty member of the Department offering the M. Tech programs.
- 8.2 **Registration of Project Work:** A candidate is permitted to register for the project work after satisfying the attendance requirement of all the subjects, both theory and practical.
- 8.3 After satisfying 8.2, a candidate has to submit, in consultation with his Project Supervisor, the title, objective and plan of action of his project work to the PRC for approval. Only after obtaining the approval of the PRC the student can initiate the Project work.
- 8.4 If a candidate wishes to change his supervisor or topic of the project, he can do so with the approval of the PRC. However, the PRC shall examine whether or not the change of topic / supervisor leads to a major change of his initial plans of project proposal. If yes, his date of registration for the project work starts from the date of change of Supervisor or topic as the case may be.
- 8.5 A candidate shall submit his project status report in four stages at least with a gap of 4 weeks between two consecutive stages for M. Tech programs and shall submit his / her project status report in two stages at least with a gap of 4 weeks between two consecutive stages.

- 8.6 The work on the project shall be initiated at the beginning of the II year and the duration of the project is two semesters for M. Tech program. A candidate is permitted to submit Project Thesis only after successful completion of all theory and practical courses (no backlogs) with the approval of PRC not earlier than 40 weeks from the date of registration of the project work. For the approval of PRC the candidate shall submit the draft copy of thesis to the Head of the Department and make an oral presentation before the PRC.
- 8.7 After approval from the PRC, the soft copy of the thesis should be submitted to the College for ANTI-PLAGIARISM for the quality check and the plagiarism report should be included in the final thesis. If the copied information is less than 24%, then only thesis will be accepted for submission.
- 8.8 Three copies of the Project Thesis certified by the supervisor shall be submitted to the College.
- 8.9 The thesis shall be evaluated by one examiner selected by the college. For this, the Head of the Department shall submit a panel of 5 examiners i.e., eminent persons with Ph. D or should have guided at least 5 M.Tech projects or should have been working in an R&D organization at the level of not less than Scientist-C, with the help of the guide concerned. The Principal will select one of the examiners and thesis will be sent for evaluation. If the report is favorable, the Head of the Department must organize for viva-voce examination.
- 8.10 If the report of the examiner is not favorable, the candidate shall revise and resubmit the Thesis, in the time frame as decided by the PRC. If the report of the examiner is unfavorable again, the thesis shall be summarily rejected. Then the candidate has to work on the thesis once again and shall submit to the PRC for its evaluation and further action on the matter.
- 8.11 For M.Tech Project Evaluation (Viva Voce) in II Year II Semester there are external marks of 70 and with 30 marks internal for 7 credits.
- 8.12 Project Viva-Voce examination shall be conducted by a board consisting of the Supervisor, Head of the Department and the external examiner who adjudicated the Thesis. Candidate has to secure minimum of 50% marks in Project Evaluation (Viva-Voce) examination.
- 8.13 If the candidate fails to secure at least 40% in the external examination and 50% in the sum total of internal and external examinations candidate is declared to be failed and the candidate has to reappear for the Viva-Voce examination only after 3 months. In the reappeared examination also, the candidate fails to fulfill the minimum qualifying requirements, he / she will not be eligible for the award of the degree.
- 8.14 The Head of the Department shall coordinate and make arrangements for the conduct of Project Viva- Voce examination.

9.0 Re-Admission:

9.1 Re-Admission for Discontinued Student:

A student, who has discontinued the M.Tech degree program due to any reason whatsoever, may be considered for 'readmission' into the same degree program (with the same specialization) with the academic regulations of the batch into which he gets readmitted, with prior permission from the authorities concerned.

9.2 If a student is detained due to shortage of attendance in any semester, he / she may be permitted to re-register for the same semester(s).

9.3 A candidate shall be given one chance to re-register for a maximum of two subjects, if the internal marks secured by a candidate are less than 50% and failed in those subjects. A candidate must re-register for failed subjects within four weeks of commencement of the class work and secure the required minimum attendance. In the event of the student taking this chance, his Continuous Internal Evaluation (internal) marks and Semester End Examination marks obtained in the previous attempt stand cancelled.

10.0 Examinations and Assessment - The Grading System:

10.1 Grades will be awarded to indicate the performance of each student in each Theory Subject, or Lab / Practical, or Seminar, or Technical Paper Writing or Project, etc., based on the percentage of marks obtained in CIE + SEE (Continuous Internal Evaluation + Semester End Examination, both taken together) as specified in item 7 above, and a corresponding Letter Grade shall be given.

10.2 As a measure of the student's performance, a 10-point Absolute Grading System using the following Letter Grades (UGC Guidelines) and corresponding percentage of marks shall be followed:

Percentage of Marks Secured in a subject / Course (Class Intervals)	Letter Grade (as per UGC guidelines)	Grade Points
90% and above (\square 90% , \leq 100%)	O (Outstanding)	10
Below 90% but not less than 80% (\square 80% , $<$ 90%)	A ⁺ (Excellent)	9
Below 80% but not less than 70% (\square 70% , $<$ 80%)	A (Very Good)	8
Below 70% but not less than 60% (\square 60% , $<$ 70%)	B ⁺ (Good)	7
Below 60% but not less than 50% (\square 50% , $<$ 60%)	B (above Average)	6
Below 50%	F (FAIL)	0
Absent	Ab	0

10.3 A student obtaining 'F' Grade in any Subject is deemed to have 'failed' and is required to reappear as 'Supplementary Candidate' for the Semester End Examination (SEE), as and when conducted. In such cases, his Internal Marks (CIE Marks) in those subjects will remain as obtained earlier.

10.4 If a student has not appeared for the examinations, 'Ab' Grade will be allocated to him for any subject and shall be considered 'failed' and will be required to reappear as 'Supplementary Candidate' for the Semester End Examination (SEE), as and when conducted.

10.5 A Letter Grade does not imply any specific marks percentage; it is only the range of percentage of marks.

10.6 In general, a student shall not be permitted to repeat any Subject (s) only for the sake of 'Grade Improvement' or 'SGPA/ CGPA Improvement'.

10.7 A student earns Grade Point (GP) in each Subject, on the basis of the Letter Grade obtained by him in that Subject / Course. The corresponding 'Credit Points' (CP) is computed by multiplying the Grade Point with Credits for that particular Subject / Course.

$$\text{Credit Points (CP)} = \text{Grade Point (GP)} \times \text{Credits For a Course}$$

10.8 The student passes the Subject / Course only when he gets GP \square 6 (B Grade or above).

10.9 The Semester Grade Point Average (SGPA) is calculated by dividing the sum of Credit Points (\square CP) secured from ALL subjects / courses registered in a semester, by the total number of Credits registered during that semester. SGPA is rounded off to TWO decimal places. SGPA is thus computed as

$$SGPA = \frac{\sum_{i=1}^n C_i G_i}{\sum_{i=1}^n C_i}$$

$$CGPA = \frac{\sum_{j=1}^M C_j G_j}{\sum_{j=1}^M C_j}$$

For each Semester

where 'i' is the subject indicator index (taking into account all subjects in a semester), 'N' is the no. of subjects 'REGISTERED' for the semester (as specifically required and listed under the course structure of the parent Department), 'C_{iii}' is the no. of Credits allotted to the ith subject, and 'G_i' represents the Grade Points (GP) corresponding to the Letter Grade awarded for that ith subject.

10.10 The Cumulative Grade Point Average (CGPA) is a measure of the overall cumulative performance of a student over all semesters considered for registration. The CGPA is the ratio of the Total Credit Points secured by a student in ALL registered courses in ALL semesters, and the Total Number of Credits registered in ALL the semesters. CGPA is rounded off to TWO decimal places. CGPA is thus computed from the I Year second semester onwards, at the end of each semester, as per the formula

$$CGPA = \{ \sum_{j=1}^M C_j G_j \} / \{ \sum_{j=1}^M C_j \} \dots\dots \text{For all 'S' Semesters registered}$$

(ie., upto and inclusive of 'S' Semesters, where S ≥ 2),

where 'M' is the TOTAL no. of subjects (as specifically required and listed under the course structure of the parent Department) the student has 'REGISTERED' for from the 1st semester onwards upto and inclusive of the semester 'S' (obviously M > N), 'j' is the subject indicator index (taking into account all subjects from 1 to 'S' semesters), 'C_{ij}' is the no. of credits allotted to the jth subject, and 'G_j' represents the Grade Points (GP) corresponding to the Letter Grade awarded for that jth subject. After registration and completion of I Year I Semester however, the SGPA of that semester itself may be taken as the CGPA, as there are no cumulative effects.

Illustration of calculation of SGPA

Course/Subject	Credits	Letter Grade	Grade points	Credit Points
Course 1	4	A	8	4*8 = 32
Course 2	4	O	10	4*10 = 40
Course 3	4	B	6	4*6 = 24
Course 4	3	B	6	3*6 = 18
Course 5	3	A+	9	3*9 = 27
Course 6	3	B	6	3*6 = 18
	21			159

$$SGPA = 159/21 = 7.57$$

Illustration of calculation of CGPA

Semester	Credits	SGPA	Credits * SGPA
Semester I	24	7	24*7 = 168
Semester II	24	6	24*6 = 144
Semester III	24	6.5	24*6.5 = 156
Semester IV	24	6	24*6 = 144
	96		612

$$CGPA = 612/96 = 6.37$$

11.0 Award of Degree and Class:

11.1 If a student who registers for all the specified Subjects/ Courses as listed in the Course Structure,

satisfies all the Course Requirements, and passes the examinations prescribed in the entire PG Programme (PGP), and secures the required number of 68 Credits (with CGPA ≥ 6.0), shall be declared to have 'QUALIFIED' for the award of the M. Tech. Degree in the chosen Branch of Engineering and Technology with the specialization that he was admitted into.

I. 11.2 Award of Class:

11.2.1 Award of degree marks equivalent to the computed final CGPA, the following % of marks = (final CGPA – 0.5) x 10

11.2.2 A student who registers for all specified subjects / courses as listed in the course structure and secures the total number of credits (with CGPA ≥ 6), within two academic years from the date of commencement of first academic year, shall be declared to have qualified for the award of M. Tech. degree in the chosen branch of engineering as selected at the time of admission.

11.2.3 A student who qualifies for award of degree as listed in item 11.2.2 shall be placed in the following classes.

11.2.4 Students with final CGPA (at the end of PG program) 8.00 and above and fulfilling the following conditions.

i) Should have passed all the subjects /courses in “first appearance” within the first 4 academic years (or 8 sequential semesters) from the date of commencement of first year first semester.

ii) Should have secured a CGPA 8.0 at the end of each of semesters, starting from first year first semester onwards.

iii) Should not have been detained or prevented from writing the end semester examinations in any semester due to shortage of attendance or any other reason, shall be placed in “FIRST CLASS WITH DISTINCTION”, otherwise FIRST CLASS only.

11.3 Students with final CGPA (at the end of the under graduate programme), ≥ 6.75 but ≤ 8.00 shall be placed in FIRST CLASS.

11.4 Students with final CGPA (at the end of under graduate programme) ≥ 6 but ≤ 6.75 , shall be placed in “SECOND CLASS”.

11.5 Students fulfilling the conditions listed under item 11.2.4 alone will be eligible for award of “University rank” and “gold medal”.

11.6 A student with final CGPA (at the end of the PGP) < 6.00 shall not be eligible for the Award of Degree.

12.0 Withholding of Results:

If the student has not paid the dues, if any, to the University / Institute or if any case of indiscipline is pending against him, the result and degree of the student will be withheld and he will not be allowed into the next semester.

13.0. Transitory Regulations:

13.1 A student who has been detained in any semester of I Year of A15 / A17 Regulations due to lack of attendance, shall be permitted to join the same semester of I Year of A19 Regulations and he is required to complete the study of M.Tech programme within the stipulated period of four academic years from the date of first admission in I Year I semester. The A19 Academic Regulations under which a student has been readmitted shall be applicable to that student from that semester.

13.2 The candidate who fails in any subject under A15 / A17 regulations will be given two chances to pass the same subject in the same regulations; otherwise, he has to identify an equivalent subject and fulfill the academic requirements of that subject as per A19 Academic Regulations.

13.3 For student readmitted to A19 Regulations, the maximum credits that a student acquires for the award of the degree, shall be the sum of the total number of credits secured in A15 / A17 regulations of his / her study including A19 Regulations.

13.4 If a student readmitted to A19 Regulations, has any subject with 80% of syllabus common with his / her previous regulations, that particular subject in A19 regulations will be substituted by another subject to be suggested by the concerned Chairman of the Board of Studies of the Department to which the student belongs to.

14.0 General:

- 14.1 **Credit:** A unit by which the course work is measured. It determines the number of hours of instructions required per week. One credit is equivalent to one hour of teaching (lecture or tutorial) or two hours of practical work / field work per week.
- 14.2 **Credit Point:** It is the product of grade point and number of credits for a course.
- 14.3 Wherever the words “he”, “him”, “his”, occur in the regulations, they shall include “she”, “her”.
- 14.4 The academic regulation should be read as a whole for the purpose of any interpretation.
- 14.5 In case of any doubt or ambiguity in the interpretation of the above rules, the decision of the **University / College Academic Council** is FINAL.
- 14.6 **The University / College Academic Council** may change or amend the academic regulations or syllabi at any time and the changes or amendments made shall be applicable to all the students with effect from the dates notified by the **University / College Academic Council**.

MALPRACTICES RULES DISCIPLINARY ACTION FOR / IMPROPER CONDUCT IN EXAMINATIONS

S.No	Nature of Malpractices/Improper Conduct	Punishment
	If the candidate:	
1.(a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject to the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination).	Expulsion from the examination hall and cancellation of the performance in that subject only.
(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.

2.	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject to the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that Semester/year. The Hall Ticket of the candidate is to be cancelled.
3.	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred and forfeits the seat. The performance of the original candidate, who has been impersonated, shall be cancelled in all the subjects of the examination (including practicals and project work) already appeared and shall not be allowed to appear for examinations of the remaining subjects of that semester / year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him.
4.	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester / year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.

5.	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that subject.
6.	Refuses to obey the orders of the Chief Superintendent / Assistant Superintendent / any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in charge or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer-in- charge, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester / year. The candidates also are debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case is registered against them.
7.	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester / year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.

8.	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester / year. The candidate is also debarred and forfeits the seat.
9.	If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	In case of student of the college, expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester / year. The candidate is also debarred and forfeits the seat. Person(s) who do not belong to the College will be handed over to police and, a police case will be registered against them.
10.	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester / year.
11.	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester / year examinations.
12.	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the University for further action to award suitable punishment.	

Malpractices identified by squad or special invigilators:

1. Punishments to the candidates as per the above guidelines.
2. Punishment for institutions: (if the squad reports that the college is also involved in encouraging malpractices)
 - (i) A show cause notice shall be issued to the college.
 - (ii) Impose a suitable fine on the college.
 - (iii) Shifting the examination centre from the college to another college for a specific period of not less than one year

M.Tech. (Digital Systems & Computer Electronics)
Course Structure and Syllabus
Academic Regulations: 2019-20

I YEAR - I Semester

Sl. No.	Code	Subject	L	T	P	Credits	CIE	SEE
1.	7U101	Digital System Design	2	1	-	3	30	70
2.	7U102	Advanced Microprocessors and Microcontrollers	2	1	-	3	30	70
3.	7U103	VLSI Technology and Design	3	1	-	4	30	70
4.	7U104	Advanced Data Communications	2	1	-	3	30	70
5.		Program Elective1	3	-	-	3	30	70
6.	7HC18	Audit course-1:English for research paper writing(Grade Evaluation)	2	-	-	0	30	70
							Grade Evaluation	
7.	7U110	Research Methodologies and IPR	2	-	-	2	30	70
8.	7U111	VLSI Technology and Design Lab	-	-	4	2	30	70
9.	7U113	Technical Seminar-1	-	-	2	1	100	-
Total			16	4	6	21	340	560

I YEAR - II Semester

Sl. No.	Code	Subject	L	T	P	Credits	CIE	SEE
1.	7U201	Advanced Computer Architecture	2	1	-	3	30	70
2.	7U202	Low Power VLSI Design	3	1	-	4	30	70
3.	7U203	Embedded Real Time Operating systems	3	-	-	3	30	70
4.	7HC19	Audit Course 2: (Ethics, Moral, Gender sensitization & Yoga)	2	-	-	0	30	70
							Grade Evaluation	
5.		Program Elective2	3	-	-	3	30	70
6.		Program Elective3	3	-	-	3	30	70
7.	7U211	Embedded Systems Lab	-	-	4	2	30	70
8.	7U212	Technical Seminar-2	-	-	2	1	100	-
9.	7U213	Comprehensive Viva Voce	-	-	2	1	30	70
10.	7U214	Mini project with seminar	*Evaluation in II year I sem					
Total			16	2	8	20	340	560

M.Tech. (Digital Systems & Computer Electronics)

Course Structure and Syllabus

Academic Regulations: 2019-20

II YEAR – I Semester

Sl. No.	Code	Subject	L	T	P	Credits	CIE	SEE
1.	7U301	Design of Fault Tolerant Systems	3	-	-	3	30	70
2.		Open Elective	3	-	-	3	30	70
3.	7U302	Mini Project with Seminars (Project Conducted in summer)	-	-	6	3	30	70
4.	7U303	Main Project Phase– I with Seminars	-	-	10	5	30	70
Total			6	0	16	14	120	280

II YEAR – II Semester

Sl. No.	Code	Subject	L	T	P	Credits	CIE	SEE
1.	7U401	Main Project Phase-2 and Seminar	-	-	12	6	30	70
2.	7U402	Dissertation and Defense viva	-	-	-	7	30	70
Total			0	0	12	13	60	140

L - Lectures; T = Tutorial; P = Practical; C = Credits
CIE: Continuous Internal Evaluation SEE: Semester End Exam Program Elective I

7U105 Advanced Digital Signal Processing
7U106 Embedded System design
7U107 Hardware Description Languages and FPGA Based Design
7U108 CMOS Analog Integrated circuit design
7U109 Hardware- Software Co-Design

Program Elective2

7U204 Wireless Communications & Networks
7U205 Image and Video Processing
7U206 CPLD & FPGA Architectures and Applications
7U207 CMOS Digital Integrated circuit design
7U208 Adhoc & Wireless Sensor Networks

Program Elective3

7U209 MIMO OFDM Systems
7U210 Digital Signal Processors and Architectures
7U215 Internet of Things
7U216 System on Chip Architecture
7U217 CMOS Analog & Mixed Signal Design

Open Elective

7ZC03 Banking Operation, Insurance and Risk Management
7ZC13 Entrepreneurship and Innovation
7P307 Network Security and cryptography
7X336 Fundamentals of Renewable Energy Sources
7ZC31 Business Analytics
7ZC32 Cost Management of Engineering Projects

**I Year -I Sem M.Tech. (DSCE)
DIGITAL SYSTEM DESIGN**

Code : 7U101

L T P C
2 1 - 3

a	b	c	d	e	f	g	h	i	j	k
x	X		X							X

After studying this course, the students will be able to

1. Explore the implementation of digital circuits using Programmable Devices such as PLA, PAL, ROM and FPGAs.
2. Understand the representation and implementation of sequential circuit with State Machine Charts, explained with examples.
3. Explore the importance and design aspects of Design for Testability.
4. Demonstrate different test pattern generation techniques to detect faults in combination circuits.
5. Describe the various Techniques of fault diagnosis in sequential circuits.
6. Explore the concepts of PLA minimization and PLA Testing.

Unit-I: Designing with Programmable Logic Devices

Designing with Read only memories – Programmable Logic Arrays – Programmable Array logic – Sequential Programmable Logic Devices – Design with FPGA’s– Using a One-hot state assignment, State transition table- State assignment for FPGA’s - Problem of Initial state assignment for One –Hot encoding - State Machine charts – Derivation of SM Charts – Realization of SM charts – Design Examples –Serial adder with Accumulator - Binary Multiplier – Dice Game controller – Binary Divider – Control logic for Sequence detector – Realization with Multiplexer – PLA – PAL.

Unit-II: Fault Modeling

Logic Fault model – Fault detection & Redundancy- Fault equivalence and fault location –Fault dominance – Single stuck at fault model – Multiple stuck at fault models –Bridging fault model
Fault diagnosis of combinational circuits by conventional methods – Path sensitization techniques, Boolean Difference method – Kohavi algorithm, Test Algorithms- D-Algorithm.

Unit-III: Test Pattern Generation

Random testing, Transition count testing, Exhaustive Testing and Pseudo Random Testing. Signature analysis and test bridging faults.

Unit-IV: Fault Diagnosis in Sequential Circuits

Circuit Test Approach, Transition Check Approach - State identification and fault detection experiment, Machine identification, Design of fault detection experiment.

Unit-V: PLA Minimization and Testing

PLA Minimization – PLA folding, Fault model in PLA, Test generation and Testable PLA Design.

Unit-VI: Minimization and Transformation of Sequential Machines

The Finite state Model – Capabilities and limitations of FSM – State equivalence and machine minimization – Simplification of incompletely specified machines. Fundamental mode model – Flow table – State reduction – Minimal closed covers – Races, Cycles and Hazards.

TEXT BOOKS:

1. Fundamentals of Logic Design – Charles H. Roth, 5th ed., Cengage Learning.
2. Digital Systems Testing and Testable Design – Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman- John Wiley & Sons Inc.
3. Switching and Finite Automata Theory – Z. Kohavi , 2nd ed., 2001, TMH
4. Logic Design Theory – N. N. Biswas, PHI

REFERENCES :

1. Digital Design – Morris Mano, M.D.Ciletti, 5^{T^h} Edition, PHI.
2. Digital Circuits and Logic Design –Samuel C. Lee, PHI

I Year – I Sem. M.Tech. (DSCE)

ADVANCED MICROPROCESSORS AND MICROCONTROLLERS

Code: 7U102

L **T** **P** **C**
2 **1** **-** **3**

a	b	c	d	e	f	g	h	i	j	k
X	X	X		X	X			X		X

After studying this course, the students will be able to

1. Understand the architecture, interfacing , instruction set and programming of 8086 microprocessor.
2. Understanding of high end Processors of X86 family, Multi-tasking and Multi-user Operating System.
3. Understanding the interfacing, interrupts, DMA, and working of cache memory, co-processors.
4. Understanding basic architecture and development tools of ARM Processor.
5. Understanding of assembly language programmed and High Level Language support provided by ARM Processor.
6. Understanding the applications of microprocessor, microcontrollers, and ARM Processor and features of some standard serial interfaces.

UNIT-I

8086 microprocessor family overview, 8086 Internal Architecture, memory interfacing constructing the machine codes for 8086, Introduction to programming the 8086, writing programmes with Assembler, Assembly Language program development tools.

UNIT-II

The 80486 and Pentium processors – The Intel 80286 microprocessor, The Intel 80386 32-Bit microprocessor architecture, The Intel 80486 microprocessor and pentium processor architecture concept of multiuser / multitasking operating system.

UNIT-III

Interfacing to 8086 microprocessor, 8086 Interrupts and Interrupt applications, Digital Interfacing, Analog interfacing and Industrial Control, DMA, Cache Memory and co-processors.

UNIT-IV

Introduction to Broad COM Processor Architecture: Architecture of BCM 2837 Processor

UNIT-V

LINUX Building Porting-Raspberry PI, Programs on Sensors, ADC, Serial Communication.

UNIT-VI

Atmel AVR Micro Controllers: Architecture, Introduction to Aurdino, Working with Aurdino Simple Programs.

TEXT BOOKS:

1. Microprocessors and Interfacing by DOUGLAS V HALL, Revised Second Edition, McGraw-Hill
2. Design with PIC microcontroller by Jhon B Peatman. Pearson education

Web Link:

1. <https://www.raspberrypi.org>
2. www.avr-tutorials.com
3. www.atmel.com

REFERENCES:

1. Embedded System Design, Frank Vahid, Tony Givargis, John Wiley.
2. Microcontrollers, Raj Kamal, Pearson Education.
3. An Embedded Software Primer, David E. Simon, Pearson Education.

**I Year – I Sem. M.Tech. (DSCE)
VLSI TECHNOLOGY & DESIGN**

Code: 7U103

L	T	P	C
3	1	-	4

a	b	c	d	e	f	g	h	i	j	k
X	X	X		X						

After studying this course, the students will be able to

1. Understand the fabrication processes and electrical properties of various MOSFET's, their advantages and disadvantages.
2. Able to draw the Layout diagrams and Stick diagrams for CMOS gates and Circuits etc. Also understand about the design rules required during drawing of Layout diagrams and Stick diagrams.
3. Understand about various alternative gate circuits and able to analyze delay and power dissipation in them.
4. Understand and analyse various delays and power consumption in the combinational circuits. Student also able to test various combinational gates and circuits for faults.
5. Understand the need of clocking disciplines required for proper operation of sequential systems and also able to analyse various delays and power consumption in the sequential circuits.
6. Understand the floor planning methods, power, clock distribution and off-chip connections of a chip.

Unit – I:

REVIEW OF MICROELECTRONICS AND INTRODUCTION TO MOS TECHNOLOGY: MOS, CMOS, BiCMOS Technologies.

BASIC ELECTRICAL PROPERTIES OF MOS AND BICMOS CIRCUITS: I_{ds} versus V_{ds} relationships, MOS Transistor Threshold Voltage V_t , MOS Transistor Transconductance(g_m) and Output Conductance(g_{ds}), Pass Transistor, nMOS Inverter, Determination of pull-up to pull down ratio(Z_{pu}/Z_{pd}) for an nMOS inverter driven by another nMOS inverter, Determination of pull-up to pull down ratio(Z_{pu}/Z_{pd}) for an nMOS inverter driven through one or more pass transistors, Alternative forms of Pull-Up, The CMOS Inverter, Latch-up in CMOS circuits, Bi CMOS Inverter.

Unit – II:

MOS TRANSISTOR PARASITICS: MOS Transistor circuit model.

LAYOUT DESIGN AND RULES: MOS Layers, Stick diagrams, Layout diagrams, Design rules for wires (nMOS and CMOS), ' λ ' based design rules, Transistor Design rules(nMOS, pMOS and CMOS), Vias, cut, Design rules for Contacts in NMOS ckts, Buried and butting contacts.

Unit – III:

LOGIC GATES: Static Complementary Gates-Gate structures, Logic levels, Delay and Transition time, Power consumption, The Speed-Power product, Driving large loads; Alternative Gate circuits-Pseudo nMOS logic, DCVS logic, Domino logic, Low power gates.

INTERCONNECTS: Estimation of Resistance, Capacitance and Inductance parasitics, Delay through Resistive interconnects-Lumped model, Lumped RC Tree model, Lumped RC ladder model, Distributed RC ladder model; Delay through Inductive interconnect-Transmission line model, Cross-talk between RC wires.

Unit – IV:

COMBINATIONAL LOGIC NETWORKS: Standard Cell Based Layout Design, Layout of Full Adder, Left edge algorithm, Combinational Network delay-Fanout delay, Path delay, delay due to false path, Transistor sizing, Cross-talk minimization, Power optimization, Combinational logic Testing-Gate Testing, Network testing.

Unit –V:

SEQUENTIAL SYSTEMS: Latches and Flip-Flops-Latch, Flip-Flop, Setup and Hold times, Dynamic Latch circuit, Multiplexed Dynamic Latch circuit, Recalculating Static latch circuit, Clocked inverter, D-Latch built from

clocked inverters, SR Flip-Flop, D-Flip-Flop; Sequential systems and Clocking disciplines-Clocking rule1, rule2, One phase systems for FFs, Two phase systems for Latches, Advanced clocking Analysis; Sequential system Design-Designing of one bit counter, Designing of a 01 string recognizer, State assignment-Encoding a Shift register, How state codes affect delay, Power optimization, testing-LSSD.

Unit – VI:

HIGH DENSITY MEMORY ELEMENTS: Architecture of a high density memory system, ROM, Static RAM, Dual ported SRAM, One transistor Dynamic RAM, Three transistor dynamic RAM.

FLOOR PLANNING: Floor planning methods-Block placement and Channel definition, Wind mill structures, Global routing, switch box routing, Power distribution, Clock distribution.

OFF-CHIP CONNECTIONS: Packages, Power line inductance, I/O Architecture, Pad Design.

TEXT BOOKS:

1. Essentials of VLSI Circuits and Systems, K. Eshraghian, Douglas A.Pucknell, 2005, PHI.
2. Modern VLSI Design - Wayne Wolf, 3rd ed., 1997, Pearson Education.
3. Digital Integrated Circuits A Design Perspective – Jan M.Rabaey, Ananta Chandrakasan, Borivoje Nikolic, Pearson Education

REFERENCES:

1. Principles of CMOS VLSI Design A System Perspective – Neil H.E.Weste, K. Eshraghian, Addison-Wesley Publishing Company.
2. Introduction to VLSI Circuits and Systems – John Uyemura, John Willey & Sons, Inc
3. VLSI design techniques for Analog and Digital Circuits – Randall L.Geiger, Phillip E.Allen, Noel R.StraderMcGraw-Hill Company
4. Application Specific Integrated circuits – Sabastian Smith, Pearson Education.

**I Year -I Sem M.Tech.(DSCE)
ADVANCED DATA COMMUNICATIONS**

Code: 7U104

								L	T	P	C
								2	1	-	3
a	b	c	d	e	f	g	h	i	j	k	
X	X	X	X					X			

After studying this course, the students will be able to

1. Describe and determine the performance of different digital modulation techniques for digital data transmission over the channel.
2. Describe data communication system model and different networks for transmission of digital data with different transmission modes and rates.
3. Describes the different error detection and correction schemes for transmission of digital information over the channel.
4. Describes the functions of Data Link control and design formats of various Data Link Protocols.
5. Describes different switching and multiplexing techniques for transmission of digital data.
6. Describe and determine the performance of Random access, controlled access and channelization protocols.

Unit-I:

Digital Modulation: Introduction, Information Capacity Bits, Bit Rate, Baud, and M-ARY Coding, ASK, FSK, PSK, QAM, BPSK, QPSK, 8PSK, 16PSK, 8QAM, 16QAM, DPSK – Methods, Band Width Efficiency, Carrier Recovery, Clock Recovery.

Applications: Ethernet

Unit -II:

Basic Concepts of Data Communications, Interfaces and Modems: Data Communication- Components, Networks, Distributed Processing, Network Criteria- Applications, Protocols and Standards, Standards Organizations- Regulatory Agencies, Line Configuration- Point-to-point- Multipoint, Topology- Mesh- Star- Tree- Bus- Ring- Hybrid Topologies, Transmission Modes- Simplex- Half duplex- Full Duplex, Categories of Networks- LAN, MAN, WAN and Internetworking, Digital Data Transmission- Parallel and Serial, DTE- DCE Interface- Data Terminal Equipment, Data Circuit- Terminating Equipment, Standards EIA 232 Interface, Other Interface Standards, Modems- Transmission Rates.

Unit-III:

Error Detection and Correction: Types of Errors- Single- Bit Error, CRC (Cyclic Redundancy Check)- Performance, Checksum, Error Correction- Single-Bit Error Correction, Hamming Code, convolution codes.

Unit-IV:

Data link Control: Stop and Wait, Sliding Window Protocols.

Data Link Protocols: Asynchronous Protocols, Synchronous Protocols, Character Oriented Protocol- Binary Synchronous Communication (BSC) - BSC Frames- Data Transparency, Bit Oriented Protocols – HDLC, Link Access Protocols. Byte oriented protocol-PPP

Unit-V:

Switching: Circuit Switching- Space Division Switches- Time Division Switches- TDM Bus- Space and Time Division Switching Combinations- Public Switched Telephone Network, Packet Switching- Datagram Approach- Virtual Circuit Approach- Circuit Switched Connection Versus Virtual Circuit Connection, Message Switching.

Multiplexing: Time Division Multiplexing (TDM), Synchronous Time Division Multiplexing, Digital Hierarchy, Statistical Time Division Multiplexing.

Unit-VI:

Multiple Access: Random Access, Aloha- Carrier Sense Multiple Access (CSMA)- Carrier Sense Multiple Access with Collision Detection (CSMA)- Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA), Controlled Access- Reservation- Polling- Token Passing, Channelization- Frequency- Division Multiple Access (FDMA), Time - Division Multiple Access (TDMA), - Code - Division Multiple Access (CDMA).

Applications: *GSM and WCDMA.*

TEXT BOOKS:

1. Data Communication and Computer Networking - B. A.Forouzan, 3rd ed., 2008, TMH.
2. Advanced Electronic Communication Systems - W. Tomasi, 5 ed., 2008, PEI.

REFERENCES:

1. Data Communications and Computer Networks - Prakash C. Gupta, 2006, PHI.
 2. Data and Computer Communications - William Stallings, 8th ed., 2007, PHI.
 3. Data Communication and Tele Processing Systems - T. Housely, 2nd Edition, 2008, BSP.
 4. Data Communications and Computer Networks- Brijendra Singh, 2nd ed., 2005, PHI.
- Telecommunication System Engineering – Roger L. Freeman, 4th ed., Wiley-Interscience, John Wiley & Sons, 2004.

I Year – I Sem. M.Tech. (DSCE)
ADVANCED DIGITAL SIGNAL PROCESSING
(PROGRAM ELECTIVE-1)

Code : 7U105

L **T** **P** **C**
3 **-** **-** **3**

a	b	c	d	e	f	g	h	i	j	k
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After going through the course, the student will be able to

1. Compute DFT and perform Linear Filtering ,Frequency Analysis of Signals using DFT.
2. Compute the Fast Fourier using the radix, Goertzel and Chrip-z Transform Algorithms.
- 3.Design IIR Filters using Butterworth and Chebyshev Approximations, and realise Structures for IIR Systems.
4. Design FIR Filters by several methods and realise Structures for FIR Systems
- 5.Define, represent, classify, analyse and also represent Multirate signal processing and its applications
- 6.Understand and predict both forward and backward linear predictors for optimum power estimation.

Unit I

DISCRETE FOURIER TRANSFORMS: Frequency domain Sampling, Properties of DFT, Linear Filtering Methods based on the DFT,Frequency Analysis of Signals using DFT.

Unit II

FAST FOURIER TRANSFORMS: Radix-2, Radix-4, Split Radix FFT Algorithms, The Goertzel Algorithm and Chrip-z Transform Algorithm.

Unit III

DESIGN OF IIR FILTERS: Design of IIR Filters using Butterworth and Chebyshev Approximations, Structures for IIR Systems –Direct Form, Cascade, Parallel, Lattice and Lattice-Ladder Structures.

Unit –IV

DESIGN OF FIR FILTERS: Fourier series method, Windowing Techniques, Design of Digital Filters based on Least-Squares Method, Structures for FIR Systems –Direct Form, Cascade, Lattice Structures.

Unit V

MULTIRATE SIGNAL PROCESSING: Introduction, Decimation by a factor D, Interpolation by a factor I, Sampling rate conversion by a rational factor I/D, Filter design & Implementation for sampling rate conversion.

Unit VI

Linear Prediction : Forward and Backward Linear Prediction – Forward Linear Prediction, Backward Linear Prediction, Optimum reflection coefficients for the Lattice Forward and Backward Predictors. Solution of the Normal Equations: Levinson Durbin Algorithm, Schur Algorithm. Properties of Linear Prediction Filters

TEXT BOOKS

Digital Signal Processing: Principles, Algorithms and Applications - J.G.Proakis & D.G.Manolokis, 5th ed., PHI.

1. Discrete Time signal processing - Alan V Oppenheim & Ronald W Schaffer, PHI.
2. DSP – A Practical Approach – Emmanuel C.Ifeacher, Barrie. W. Jervis, 2nd ed., Pearson Education.

REFERENCE BOOKS

1. Digital Spectral Analysis with applications– S. Lawrence Marple Jr, Prentice-Hall Series in Signal Processing.
2. Modern spectral Estimation : Theory & Application – S. M .Kay, 1988, PHI.
3. Multirate Systems and Filter Banks – P.P.Vaidyanathan – Pearson Education
4. Digital Signal Processing – S.Salivahanan, A.Vallavaraj, C.Gnanapriya, 2000,TMH

**I Year – I Sem. M.Tech. (DSCE)
EMBEDDED SYSTEM DESIGN
(PROGRAM ELECTIVE-I)**

Code : 7U106

L T P C
3 - - 3

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On completion of this course you should be able to:

1. Understand the basic architecture of Embedded System and their classification.
2. Explore the architecture of ARM processor.
3. Understand the addressing modes and data processing instructions of ARM processor.
4. Understand the ARM thumb instruction set and its capabilities.
5. Use both assembly and C language based ARM programming.
6. Explore the memory management techniques in ARM.

UNIT-I

Introduction to embedded system:

Embedded system architecture, classifications of embedded systems, challenges and design issues in embedded systems, fundamentals of embedded processor and microcontrollers, CISC vs. RISC, fundamentals of VonNeuman/Harvard architectures, types of microcontrollers, selection of microcontrollers.

UNIT –II:

ARM Architecture:

ARM Design Philosophy, Registers, Program Status Register, Instruction Pipeline, Interrupts and Vector Table, Architecture Revision, ARM Processor Families.

UNIT –III:

ARM Programming Model – I:

Instruction Set: Data Processing Instructions, Addressing Modes, Branch, Load, Store Instructions, PSR Instructions, Conditional Instructions.

UNIT –IV:

ARM Programming Model – II:

Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instructions, Single-Register and Multi Register Load-Store Instructions, Stack, Software Interrupt Instructions

UNIT –V:

ARM Programming:

Simple C Programs using Function Calls, Pointers, Structures, Integer and Floating Point Arithmetic, Assembly Code using Instruction Scheduling, Register Allocation, Conditional Execution and Loops.

UNIT –VI:

Memory Management:

Cache Architecture, Polices, Flushing and Caches, MMU, Page Tables, Translation, Access Permissions, Context Switch.

TEXT BOOKS:

1. ARM Systems Developer’s Guides- Designing & Optimizing System Software – Andrew N. Sloss, Dominic Symes, Chris Wright, 2008, Elsevier.

REFERENCE BOOKS:

Embedded Microcomputer Systems, Real Time Interfacing – Jonathan W. Valvano – Brookes / Cole, 1999, Thomas Learning.

**I Year – I Sem. M.Tech.(DSCE)
Hardware Description Languages and FPGA based Design
(PROGRAM ELECTIVE-I)**

Code : 7U107

L T P C
3 - - 3

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After going through the course, the student will be able to

1. Understand the basics concepts of verilog.
2. Implementing digital designs using various types of modeling styles.
3. Understand the basic FPGA architecture and its programming.
4. Understand the FPGA design flow using EDA tools.
5. Understand the synthesis and implementation on FPGA using VHDL.
6. Understand the synthesis and implementation on FPGA using Verilog.

Unit-I

Verilog : basic concepts- Lexical conventions, data types, system tasks and compiler directives. Modules and ports. Gate level modeling- gate types, various types of gate delay specifications.

Unit-II

Data flow modeling- assignments, delays, expressions, operators, Behavioral modeling- structured procedures, procedural assignments, timing controls, conditional statements, loops, sequential and parallel blocks, generate blocks. Tasks and functions

Unit-III

FPGA Architectures and Technology. Historical background, channel type FPGA Xilinx Spartan 3E family, structured programmable array logic, programming FPGAs, benchmarking of FPGAs.

Unit-IV

Design Flow of FPGA and EDA Software: Development flow: RTL code, testbench, RTL simulation, synthesis, implementation, static timing analysis, device programming, Overview of Xilinx ISE project navigator, Xilinx Vivado System Design software flow.

Unit-V

VHDL Synthesis for FPGA Implementation.: Mapping of statements to gate assignment statements, logical, arithmetic and relational operators, vectors and slices, IF, Process, Case, Loop, Null, Wait statements. Modeling of flip-flops and latches. Modeling of FSM for synthesis. Some examples of synthesizable constructs.

Unit-VI

Verilog Synthesis for FPGA Implementation: Verilog constructs and operators, interpretation of Verilog constructs, synthesis design flow- RTL to gates, translation, un optimized intermediate representations, logic optimization, technology mapping and optimization, technology library, design constraints, optimized gate level description.

TEXT BOOKS:

- 1 S. Palnitkar, *Verilog HDL : A Guide to Digital Design and Synthesis*, PH/Pearson.
- 2 Pong P. Chu, *FPGA Prototyping by Verilog Examples* –WILEY Publications.
3. K. Coffman, *Real World FPGA Design with Verilog*, PH.

REFERENCES:

1. P.J. Ashenden, *The Designer's Guide to VHDL*, Second Edition, Morgan Kaufmann.
2. C. H. Roth, *Digital System Design with VHDL*, PWS/Brookscole.
3. R. C. Seals and G. F. Whapshott, *Programmable Logic : PLDs and FPGAs*, MH.
4. A.K. Sharma, *Programmable Logic Handbook : PLDs, CPLDs and FPGAs*, MH.

**I Year – I Sem. M.Tech.(DSCE)
CMOS ANALOG INTEGRATED CIRCUIT DESIGN
(PROGRAM ELECTIVE-I)**

Code : 7U108

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Course Objectives:

- To understand the Basic MOS Device Physics.
- To understand the operation of different types of single stage amplifiers, current sources and current sinks and voltage references.
- To understand the analysis and design of analog circuits with emphasis on CMOS technology.
- To gain knowledge in designing of advanced operational amplifiers.
- To understand the fundamentals of comparators.

UNIT -I: MOS Devices and Modeling:

The MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT -II: Analog CMOS Sub-Circuits:

MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT -III: CMOS Amplifiers:

Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

UNIT -IV: CMOS Operational Amplifiers:

Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power-Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OP Amp.

UNIT -V: Comparators:

Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

UNIT IV : ADC/DAC ARCHITECTURES

DAC Performance Metrics, Reference Multiplication And Division, Switching And Logical Functions Of DACs, Current Steering Architectures, DAC Performance Metrics, Flash ADC Architecture, Gray Encoding, Thermometer Encoding And Metastability.

TEXT BOOKS:

1. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
2. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.

REFERENCE BOOKS:

1. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edn, 2013.
2. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition.
3. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI.

**I Year – I Sem. M.Tech.(DSCE)
HARDWARE- SOFTWARE CO-DESIGN
(PROGRAM ELECTIVE-1)**

Code: 6T103

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After going through the course, the student will be able to

- 1: Able to understand models, architecture, methodology and languages for co-design. Hardware-Software algorithms are studied
- 2: To understand Prototyping and emulation techniques, environments, future developments, architecture Specialization techniques and system communication infrastructure
- 3: Study of target architectures
- 4: Study of compilation technologies and tools for embedded processor architectures
- 5: Able to understand computational model, interfacing components, design and implementation verification, verification tools
- 6: Study of design representation for system level synthesis, system level specification languages

Unit –I

CO- DESIGN ISSUES

Co- Design Models, Architectures, Languages, a Generic Co-design Methodology.

CO- SYNTHESIS ALGORITHMS

Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

Unit –II

PROTOTYPING AND EMULATION

Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

Unit -III

TARGET ARCHITECTURES

Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

Unit – IV

COMPILATION TECHNIQUES AND TOOLS FOR EMBEDDED PROCESSOR ARCHITECTURES

Modern embedded architectures, embedded software development needs, compilation technologies practical consideration in a compiler development environment.

Unit – V

DESIGN SPECIFICATION AND VERIFICATION

Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

Unit – VI

LANGUAGES FOR SYSTEM – LEVEL SPECIFICATION AND DESIGN-I

System – level specification, design representation for system level synthesis, system level specification languages

LANGUAGES FOR SYSTEM – LEVEL SPECIFICATION AND DESIGN-II

Heterogeneous specifications and multi language co-simulation the cosyma system and lycos system.

TEXT BOOKS

1. Hardware / software co- design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – 2009, Springer.
2. Hardware / software co- design Principles and Practice, 2002, Kluwer Academic Publishers

**I Year – I Sem. M.Tech.(DSCE)
RESEARCH METHODOLOGY AND IPR**

Code: 7U110

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Course Outcomes:

At the end of this course, students will be able to

- Understand research problem formulation.
- Analyze research related information
- Follow research ethics
- Understand that today’s world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.
- Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.
- Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

UNIT – I Introduction:

Objective of Research, Definition and Motivation, Types of Research, Research Approaches, Steps in Research Process, Criteria of Good Research, and Ethics in Research.

Research Formulation and Literature Review: Problem Definition and Formulation; Literature Review; Characteristics of Good Research Question; Literature Review Process.

UNIT - II Data Collection:

Primary and Secondary Data, Primary and Secondary Data Sources, Data Collection Methods, Data Processing, Classification of Data.

Data Analysis:

Statistical Analysis; Multivariate Analysis; Correlation Analysis; Regression Analysis; Principle Component Analysis; Samplings.

UNIT - III Research Design:

Need for Research Design; Features of a Good Design; Types of Research Designs; Induction and Deduction.

Hypothesis Formulation and Testing:

Hypothesis; Important Terms; Types of Research Hypothesis; Hypothesis Testing; Z-Test; tTest; f-Test; Making a Decision; Types of Errors; ROC Graphics.

UNIT - IV Test Procedures:

Parametric and Non Parametric Tests; ANOVA; Mann-Whitney Test; Kruskal-Wallis Test; Chi-Square Test; Multi-Variate Analysis

Presentation of the Research Work:

Business Report; Technical Report; Research Report; General Tips for Writing Report; Presentation of Data; Oral Presentation; Bibliography and References; Intellectual Property Rights; Open-Access Initiatives; Plagiarism.

UNIT - V

Law of Patents, Patent Searches, Ownership, Transfer Patentability – Design Patents – Double Patenting – Patent Searching – Patent Application Process – Prosecuting the Application, Post-issuance Actions, Term and Maintenance of Patents. Ownership Rights – Sole and Joint Inventors – Inventions Made by Employees and Independent Contractors – Assignment of Patent Rights – Licensing of Patent Rights – Invention Developers and Promoters.

Patent Infringement, New Developments and International Patent Law Direct

Unit VI

Infringement – Inducement to Infringe – Contributory Infringement – First Sale Doctrine – Claims Interpretation – Defenses to Infringement – Remedies for Infringement – Resolving an Infringement Dispute – Patent Infringement Litigation. New Developments in Patent Law

Text Books

1. Research Methodology. Methods & Technique : Kothari. C.R.
2. Intellectual Property – Copyrights, Trademarks, and Patents by Richard Stim, Cengage Learning

References

1. Practical Research : planning and Design(8th Edition) – Paul D. Leedy and Jeanne E.Ormrod.
2. A Hand Book of Education Research – NCTE 3. Methodology of Education Research – K.S. Sidhu.
4. Tests, Measurements and Research methods in Behavioural Sciences- A.K. Singh.
5. Statistical Methods- Y.P. Agarwal.
6. Methods of Statistical Analysis- P.S Grewal. 7. Fundamentals of Statistics – S.C. Gupta, V.K. Kapoor.
8. Intellectual Property Rights by Deborah E. Bouchoux, Cengage Learning.
9. Managing Intellectual Property – The Strategic Imperative, Second Edition by Vinod V.Sople, PHI Learning Private Limited.
10. Research methodology – S.S. Vinod Chandra, S. Anand Hareendran

**I Year – I Sem. M.Tech (DSCE)
VLSI Technology and Design LAB**

Code:7U111

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X		X	X	X	X			X		X				

After going through the Laboratory course, the student will be able to

1. Design, Simulate, Verify, Synthesize Various Logic gates and also implement them on FPGA Board.
2. Design, Simulate, Synthesize and Implement various Combinational Logic Circuits and verify with FPGA Board.
3. Design, Simulate, Synthesize and Implement various Sequential Logic Circuits and verify with FPGA Board.
4. Schematic design and verification of logic Gates using Back end SW tool
5. Layout design, LVS verification, DC and AC analysis using Back end SW tool.
6. Schematic design and verification of OPAMP Circuits using Back end SW tool

LIST OF EXPERIMENTS:

CYCLE 1: Combinational and Sequential Digital Circuit Design

Design the following experiments using Verilog HDL/VHDL, verify the RTL Design, perform Synthesis, Timing simulation, Implementation and verification on FPGA boards. Tools required: Front end SW tool and FPGA Boards.

1. Logic gates (Basic and Universal Gates)
2. Adders (HA, FA, Parallel Adders)
3. Decoders and Encoders
4. Multiplexers and Demultiplexers
5. Flip Flops (SR, D, JK, T)
6. Delay generation (1S, 2S etc.) and verification with LEDs
7. Seven Segment Display Interfacing
8. Synchronous Counter
9. Asynchronous Counter

CYCLE 2: VLSI Back End Design

Schematic design and verification, Layout design, LVS verification, DC and AC analysis of the following experiments. Tools required : Back end VLSI SW Tool.

1. Basic Gates (AND, OR & NOT)
2. Universal Gates (NOR / NAND)
3. Parity generators (even/odd)
4. Single stage OPAMP

**I Year -I Sem M.Tech. (DSCE)
TECHNICAL SEMINAR-1**

Code: 7U113

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Max. Marks: 100

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After Completing this course, the students will be able to

1. Identify a research topic
2. Collect literature
3. Present seminar
4. Discuss the queries

There shall be seminar presentations during I year I semester. Student shall collect the literature on a topic and critically review the literature and submit it to the Department in a report form, under the supervision of a faculty member and shall make an oral presentation before the Departmental Committee, which consists of the Head of the Department, a senior Faculty Member and the Supervisor, who will jointly evaluate the report and presentation. For each Seminar there will be only internal evaluation of 100 marks. A candidate has to secure a minimum of 50% to be declared successful.

In the First semester the report must be in the form of the review paper with a format used by IEEE / ASME etc. In the Second semester Technical Seminar in the form of Independent Review Paper must be of high quality fit for publication in a reputed conference / journal.

The evaluation format for seminar is as follows:

- Day to day evaluation by the Supervisor : 20 marks
- Final Report : 30 marks
- Presentation : 50 marks

A Student has to concentrate on the following sections while writing technical paper or presenting seminar.

Contents:

- Identification of specific topic
- Analysis
- Organization of modules
- Naming Conventions
- Writing style
- Figures
- Feedback
- Writing style
- Rejection
- Miscellaneous

REFERENCES:

Teach Technical Writing in Two Hours per Week by Norman Ramsey

For Technical Seminar the student must learn few tips from sample seminars and correcting himself, which is continues learning process

REFERENCE LINKS:

1. <http://www.cs.dartmouth.edu/~scot/givingTalks/sld001.htm>
2. <http://www.cse.psu.edu/~yuanxie/advice.htm>
3. <http://www.eng.unt.edu/ian/guides/postscript/speaker.pdf>

NOTE: A student can use any references for this process, but must be shared in classroom.

**I Year – II Sem. M.Tech.(DSCE)
ADVANCED COMPUTER ARCHITECTURE**

Code: 7U201

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After studying this course, the students will be able to

1. Describe fundamentals of computer design instruction set and memory addressing .
2. Describe pipelines ,Pipeline hazards and RISC processor .
3. Describe cache memory and virtual memory.
4. Explain instruction level parallelism and dynamic scheduling
5. Explain multiprocessors and thread level parallelism
6. Describe practical issues in interconnecting networks and design of cluster

UNIT- I: Fundamentals of Computer Design

Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, quantitative principles of computer design, Amdahl's law.

Instruction set principles and examples- Introduction, classifying instruction set- memory addressing- type and size of operands, operations in the instruction set.

UNIT – II: Pipelines

Introduction ,basic RISC instruction set ,Simple implementation of RISC instruction set, Classic five stage pipe line for RISC processor, Basic performance issues in pipelining , Pipeline hazards, Reducing pipeline branch penalties.

UNIT - III

Memory Hierarchy Design

Introduction, review of ABC of cache, Cache performance , Reducing cache miss penalty, Virtual memory.

UNIT - IV Instruction Level Parallelism the Hardware Approach

Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, high performance instruction delivery- hardware based speculation.

ILP Software Approach

Basic compiler level techniques, static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues -Hardware verses Software.

UNIT –V: Multi Processors and Thread Level Parallelism

Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – memory architecture, Synchronization.

UNIT – VI: Inter Connection and Networks

Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters.

Intel Architecture

Intel IA- 64 ILP in embedded and mobile markets Fallacies and pit falls

TEXT BOOKS:

1. John L. Hennessy, David A. Patterson, Computer Architecture: A Quantitative Approach, 3rd Edition, An Imprint of Elsevier.

REFERENCE BOOKS:

1. John P. Shen and Miikko H. Lipasti, Modern Processor Design : Fundamentals of Super Scalar Processors
2. Computer Architecture and Parallel Processing ,Kai Hwang, Faye A.Brigs., MC Graw Hill.,
3. Advanced Computer Architecture - A Design Space Approach, Dezso Sima, Terence Fountain, Peter Kacsuk ,Pearson ed.

**I Year – II Sem. M.Tech.(DSCE)
LOW POWER VLSI DESIGN**

Code: 7U202

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3 1 - 3

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After going through the course, the student will be able to

1. Understand the implications of Low Power Design on IC Fabrication.
2. Understand the various deep submicron Processes and their future trends and directions.
3. Understand and analyse various MOSFET and Bipolar models and their limitations.
4. Know, Understand the conventional CMOS and BiCMOS logic gates, able to analyse power dissipation of the CMOS Inverter and its implementation of two- i/p NOR and NAND gates. He is also able to understand the basic driver configurations of the BiCMOS logic gate associated with shunting devices for full o/p voltage swing.
5. Understand the design of various low power BiCMOS circuits for high performance at low power supply voltages.
6. Trace out the reasons for Evolution of Latches and Flip flops. He is also able to understand the quality measures for latches and Flip flops and Design perspective.

Unit I

INTRODUCTION: low power design - an over view, Low-Voltage, Low power design limitations, Silicon-on-Insulator Technology.

Unit II

MOS/BICMOS PROCESSES-TECHNOLOGY AND INTEGRATION: Introduction, The realization of BiCMOS processes-Low cost medium speed 5volts digital BiCMOS process, High performance high cost 5volts digital BiCMOS process, Twin well BiCMOS process; BiCMOS manufacturing and Integration considerations- Consideration for CMOS device structures, Process consideration for Bipolar transistors; Isolation in BiCMOS- Isolation in Bipolar transistors, Isolation in MOS transistors; Advanced isolation technologies.

Unit III

DEEP SUBMICRON PROCESSES: Polysilicon Emitter High-Performance BiCMOS Structure, Low capacitance Bipolar/BiCMOS Processes,SOI CMOS/BiCMOS VLSIs.

LOW-VOLTAGE/LOW POWER CMOS/ BICMOS PROCESSES: Low Voltage/Low Power SOI CMOS, Properties of fully depleted SOI MOSFETs, Low Voltage/Low Power Lateral BJT on SOI, Future trends and Directions of CMOS/BiCMOS processes.

Unit IV

CMOS AND Bi-CMOS LOGIC GATES: Conventional CMOS logic gates.

CONVENTIONAL BICMOS LOGIC GATES:Basic Driver configurations, Full swing with shunting devices, FS-CMBL, FS-CMBL with feedback, High performance CCBiCMOS circuit.

Unit V

LOW- VOLTAGE LOW POWER LOGIC CIRCUITS-1: BiCMOS Circuits Utilizing Lateral pnp BJTs in pMOS Structures, Merged BiCMOS Digital Circuits, Full-Swing Multi Drain/Multi Collector Complementary BiCMOS Buffers, Quasi Complementary BiCMOS Digital Circuits, Full-Swing BiCMOS/BiNMOS Digital Circuits Employing Schottky Diodes.

Unit VI

LOW- VOLTAGE LOW POWER LOGIC CIRCUITS-2: Feedback type BiCMOS Digital Circuits, High-Beta BiCMOS Digital Circuits, Transiently Saturated Full-Swing BiCMOS Digital Circuits, Bootstrapped-Type BiCMOS Digital Circuits-1.5volts Bootstrapped BiCMOS logic gate, Bootstrapped FS BiCMOS/BiNMOS Inverter, ESD-free Bi CMOS Digital Circuit.

TEXT BOOKS

1. CMOS/BiCMOS ULSI low voltage, low power by Yeo Rofail/ Gohl(3 Authors)-Pearson Education Asia
1st Indian reprint,2002

REFERENCES

1. Digital Integrated circuits , J.Rabaey PH. N.J 1996
2. CMOS Digital ICs , Sung-moKang and Yusuf Leblebici 3rd edition TMH 2003 (chapter 11)
3. VLSI DSP systems , Parhi, John Wiley & sons, 2003 (chapter 17)
4. IEEE Trans Electron Devices, IEEE J.Solid State Circuits, and other National and International Conferences and Symposia

I Year – II Sem. M.Tech.(DSCE)
EMBEDDED REAL TIME OPERATING SYSTEMS

Code: 7U203

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After going through the course, the student will be able to

1. Understand embedded systems and various options and challenges in building them.
2. Understand the Real Time Systems and various parameters of tasks and models.
3. Understand various scheduling policies.
4. Understand the constructs used for inter-process communication.
5. Understand various services provided RTOS and Micro C/O.S.-II.
6. Understand Vx WORKS O.S. and some case studies

Unit I: Introduction

Embedded systems overview, design challenges, processor technology, I.C. technology, design technology, trade-offs. Single purpose processors, optimizing custom single purpose processors and general purpose processors, ASIPS, microcontrollers and DSP processors for embedded systems.

Unit II: Real Time Systems:

Typical real time applications, Hard Vs Soft real-time systems, A reference model of Real Time Systems: Processors and Resources, Temporal Parameters of real Time Work load, Periodic task model precedence constraints and data dependency, functional parameters, Resource Parameters of jobs and parameters of resources.

Unit III: Scheduling

Commonly used Approaches to Real Time Scheduling Clock Driven, Weighted Round Robin, Priority Driven, Dynamic Vs State Systems, Effective release time and Dead lines, Offline Vs Online Scheduling. Scheduling real time tasks in multi processor and distributed systems.

Unit IV: Inter-process Communication

Inter-process Communication and Synchronization of Processes, Tasks and Threads- Multiple Process in an Application, Problem of Sharing data by multiple tasks & routines, Inter-process communication

Unit V: Real Time Operating Systems & Programming Tools

Operating Systems Services, I/O Subsystems, RT & Embedded Systems OS, Interrupt Routine in RTOS Environment

Micro C/OS-II- Need of a well Tested & Debugged RTOs, Use of μ COS-II

Unit VI: VX Works & Case Studies

Memory managements task state transition diagram, pre-emptive priority, Scheduling context switches- semaphore- Binary mutex, counting watch dogs, I/O system

Case Studies of programming with RTOS- Case Study of Automatic Chocolate Vending m/c using μ COS RTOS, case study of sending application Layer byte Streams on a TCP/IP network, Case Study of an Embedded System for a smart card.

TEXT BOOKS:

1. Embedded Systems- Architecture, Programming and Design by Rajkamal, 2nd ed., 2008, TMH.
2. Real Time Systems- Jane W. S. Liu- PHI.
3. Real Time Systems- C.M.Krishna, KANG G. Shin, 1996, TMH
4. Embedded system Design-A unified hardware/ software approach by Frank Vahid, Tony D. Givargis, Johnwiley, 2002.

REFERENCES:

1. Advanced UNIX Programming, Richard Stevens
2. VX Works Programmers Guide

I Year -II Sem M.Tech.(DSCE)
WIRELESS COMMUNICATIONS & NETWORKS
(PROGRAM ELECTIVE-2)

Code : 7U204

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Course objectives:

The objectives of this course are

- *To provide an overview of Wireless Communication networks area and its applications in communication engineering.*
- *To appreciate the contribution of Wireless Communication networks to overall technological growth.*
- *To understand the various terminology, principles, devices, schemes, concepts, algorithms and different methodologies used in Wireless Communication Networks.*

UNIT-I: Introduction to Wireless Communication Systems: Evolution of mobile radio communications, Examples of wireless communication systems, Paging systems, Cordless telephone systems, Comparison of various wireless systems.

Modern wireless communication systems: Second generation cellular networks, Third generation wireless networks, Wireless in local loop, Wireless LAN, Bluetooth and PAN.

UNIT- II: Multiple Access Techniques for Wireless Communication: Introduction to multiple access, FDMA, TDMA, Spread spectrum multiple access, Space division multiple access, Packet Radio, Capacity of cellular systems.

UNIT-III: Wireless Networking: Differences between wireless and fixed telephone networks, Development of wireless networks, Fixed network transmission hierarchy, Traffic routing in wireless networks, Wireless data services, Common channel signaling.

UNIT- IV: Mobile IP And Wireless Access Protocol: Mobile IP Operation of mobile IP, Co-located address, Registration, Tunneling, WAP Architecture-overview, WML scripts, WAP service, WAP session protocol, Wireless transaction, Wireless datagram protocol.

UNIT- V: Wireless LAN: Historical overview of the LAN industry, Evolution of the WLAN industry, Wireless home networking, IEEE 802.11, The PHY layer, MAC Layer, Wireless ATM, HYPERLAN, HYPERLAN-2, Introduction to OFDM, Blue tooth protocol Architecture.

UNIT- VI: Wireless WAN: Mechanism to support a mobile environment, Communication in the infrastructure. IS-95 CDMA forward channel, IS-95 CDMA reverse channel, Packet and frame formats in IS-95, IMT – 2000, Forward channels in W-CDMA and CDMA-2000, Reverse channels in W-CDMA and CDMA-2000, GPRS and higher data rates, Short messaging service in GPRS mobile application protocols.

Text Books:

1. Theodore S. Rappaport, “*Wireless Communications and applications*”, Pearson Education -2003.
2. Kaveh Pahlavan, Prashant Krishna Murthy, “*Principles of Wireless networks*”, Pearson Education, 2002.

Reference Books:

1. P.Nicopolitidis, M.S.Obaidat, G.I.Papadimitria, A.S. Pomportsis, “*Wireless Networks*”, John wily & sons, 2003.
2. Dr. Sunil kumar, S.manvi, M.S.Kakkasageri, ”*Wireless and Mobile Networks, Concepts and Protocols*”, Wiley India, 2010.
3. Jon W.Mark and W.Zhqung , “ *Wireless Communication and Networking* “, PHI, 2005.

**I Year -II Sem M.Tech.(DSCE)
IMAGE & VIDEO PROCESSING
(PROGRAM ELECTIVE-2)**

Code : 7U205

L T P C
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After studying this course, the students will be able to

1. Get the knowledge of the basic step in image processing system, Discrete cosine transforms and discrete wavelet transforms.
2. Differentiate image enhancement methods, different types of spatial domain and frequency domain methods.
3. Get the knowledge of point, line and edge detection, thresholding, Region based segmentation.
4. Differentiate different types of redundancies, lossy and lossy less image compression, different types of coding techniques.
5. Know the difference between analog video and digital video, different types of image formation and sampling of video signals
6. Study the different types of motion estimation techniques and application of motion estimation in video coding.

Unit I: Fundamentals of Image Processing and Image Transforms

Basic steps of Image Processing System Sampling and Quantization of an image – Basic relationship between pixels
Image Transforms: 2 D- Discrete Fourier Transform, Discrete Cosine Transform (DCT), Wavelet Transforms: Continuous Wavelet Transform, Discrete Wavelet Transforms.

Unit II: Image Enhancement

Spatial domain methods: Histogram processing, Fundamentals of Spatial filtering, Smoothing spatial filters, Sharpening spatial filters.
Frequency domain methods: Basics of filtering in frequency domain, image smoothing, image sharpening, Selective filtering.

Unit III: Image Segmentation & Compression

Image Segmentation concepts, Point, Line and Edge Detection, Thresholding and Region Based segmentation.
Image compression fundamentals - Coding Redundancy, Spatial and Temporal redundancy, Compression models: Lossy & Lossless, Huffman coding, Arithmetic coding, LZW coding, Run length coding, Bit plane coding, Transform coding, Predictive coding.

Unit IV: Basic steps of Video Processing

Analog Video, Digital Video. Time-Varying Image Formation models: Three-Dimensional Motion Models, Geometric Image Formation, Photometric Image Formation, Sampling of Video signals and filtering operations.

Unit V: 2-D Motion Estimation

Optical flow, General Methodologies, Pixel Based Motion Estimation, Block- Matching Algorithm, Mesh based Motion Estimation, Global Motion Estimation, Application of motion estimation in Video coding.

Unit VI: Three dimensional Motion Estimation & Waveform based coding

Feature based motion estimation, Direct Motion Estimation. **Block based transform coding:** over view, one dimensional unitary transform, two dimensional unitary transform, The discrete cosine transform, Bit allocation and transform coding gain , **Predictive Coding:** over view, optimal predictor design and predictive coding gain, Block based hybrid video coding.

TEXT BOOKS

1. Digital Image Processing – Gonzalez and Woods, 3rd ed., Pearson.
2. Video processing and communication – Yao Wang, Joem Ostermann and Ya–quin Zhang. 1st Ed., PH Int.

REFERENCE BOOKS

1. Digital Video Processing – M. Tekalp, Prentice Hall International

I Year – II Sem. M.Tech. (Digital Systems & Computer Electronics)
CPLD & FPGA ARCHITECTURES AND APPLICATIONS
(PROGRAM ELECTIVE-2)

Code: 7U206

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After studying this course, the students will be able to

1. Understand the classification of PLDs and Architectures of AMD and Altera Flex-10K series CPLD.
2. Understand the basic architecture of Spartan-3 FPGA architecture, Artix-7 series FPGA
3. Understand the basic design flow of FPGA using EDA Tools: Xilinx ISE project navigator, Xilinx Vivado System Design.
4. Design the Combinational logic designs with various examples.
5. Design the Sequential logic designs with various examples. Understand and explore the FSM and FSMD designs of digital systems using available EDA tools.
6. Understand and analyze the front-end designs and case studies of digital system designs using EDA tools.

Unit –I

Programmable logic : Classification of PLDs, Features, architectures of complex programmable logic devices, AMD, Altera FLEX logic-10000 series CPLD.

Unit –II

FPGA Architectures: Overview of a general FPGA device, Xilinx FPGA versions and specifications, Xilinx Spartan-3 FPGA architecture, Artix-7 series FPGA architectural features and specifications. Speed performance and in system programmability.

Unit – III

DESIGN FLOW OF FPGA AND EDA SOFTWARE: Development flow: RTL code, testbench, RTL simulation, synthesis, implementation, static timing analysis, device programming, Overview of FPGA Design flow.

Unit-IV

RTL DIGITAL DESIGNS-I: Combinational circuit designs, routing structure of conditional control constructs, implementation of if- statement and parallel case statement for priority routing network, general coding guidelines for an always block, common errors in combinational circuit codes, parameter and constant. Design example: Hexadecimal digit to seven segment LED decoder, barrel shifter, floating point adder, ALU design.

Unit-V

RTL DIGITAL DESIGNS-II: Sequential designs: HDL for D-FF, register, shift register, universal shifter, synchronous and asynchronous counter designs.
 FSM and FSMD: FSM representation, state diagram, ASM chart, Moore based designs, Mealy based designs, single RT operation, ASMD Chart and its code development, binary to BCD conversion, division circuit.

Unit - VI

Digital front-end design tools for FPGAs & ASICs. Various EDA tools – Design flow using FPGAs. Method to incorporate memory modules, HDL examples for Single and dual port RAM, ROM.

TEXT BOOKS:

1. FPGA PROTOTYPING BY VERILOG EXAMPLES –Pong P. Chu, WILEY Publications.
2. FPGA based System Design- W. Wolf, Prentice Hall, 2004.
3. Embedded Core Design with FPGAs-Zainalabedin Navabi, Tata McGraw-Hill Publications.

REFERENCES:

1. Digital Design Using Field Programmable Gate Array, P.K.Chan & S. Mourad, 1994, Prentice Hall.
2. Data sheets of Artix 7 series FPGA from Xilinx website.
3. User guide of Xilinx Vivado System Design from Xilinx Website.
4. Digital Systems Design with FPGA's and CPLDs – Ian Grout, 2009, Elsevier.

I Year – II Sem. M.Tech. (Digital Systems & Computer Electronics)
CMOS DIGITAL INTEGRATED CIRCUIT DESIGN
(PROGRAM ELECTIVE-2)

Code: 7U207

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Course Objectives:

1. Introduction to VLSI Systems
2. CMOS logic Design,
3. Combinational MOS logic circuits Circuit characterization and performance estimation
4. Combinational and sequential circuit design
5. Memory system design
6. Design methodology and tools

UNIT –I: MOS Design:

Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT –II: Combinational MOS Logic Circuits:

MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates , AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT –III: Sequential MOS Logic Circuits:

Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flipflop.

UNIT –IV: Dynamic Logic Circuits:

Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

UNIT –V: Semiconductor Memories:

Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory- NOR flash and NAND flash.

UNIT –VI: Timing Issues In Digital Circuits : Introduction, Timing Classification Of Digital Systems , Synchronous Design – An In depth Perspective , Self-Timed Circuit Design , Synchronizers And Arbiters .

Designing Arithmetic Building Blocks : Introduction , Datapaths In Digital Processor Architectures , The Adder, The Multiplier, The Shifter.

TEXT BOOKS:

1. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Digital Integrated Circuits – A Design Perspective, Jan M. Rabaey, AnanthaChandrakasan, BorivojeNikolic, 2nd Ed., PHI.

**I Year – II Sem. M.Tech.(DSCE)
AD HOC AND WIRELESS SENSOR NETWORKS
(PROGRAM ELECTIVE-2)**

Code: 7U208

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By the end of this course, students will be able to

1. *Understand basics of Ad hoc Wireless Networks, MAC protocols for Ad hoc Wireless Networks.*
2. *Understand Routing protocols for Ad hoc Wireless Networks.*
3. *Understand Wireless sensor Networks.*
4. *Understand different routing techniques.*
5. *Understand the basics and issues of Wireless Sensor Networks.*
6. *Understand the difference and details of Random vs. structured Wireless Sensor Networks.*

Unit I

Ad Hoc Networks:

Characteristics and Applications of Ad hoc Networks, Routing – Need for routing and routing, classifications, Table Driven Routing Protocols, Source Initiated On-Demand

Unit II

Routing Protocols, Hybrid, Protocols – Zone Routing, Fisheye Routing, LANMAR for MANET with group mobility, Location Added Routing, Distance Routing Effects, Microdiscovery and Power Aware Routing.

Unit III

Wireless Sensor Networks:

Wireless Sensor Networks, DARPA Efforts, Classification, Fundamentals of MAC, Flat routing.

Unit IV

Routing:

Directed Diffusion, SPIN, COGUR, Hierarchical Routing, Cluster base routing,

Unit V

Scalable Coordination, LEACH, TEEN, APTEEN and Adapting to the dynamic nature of Wireless Sensor Networks.

Unit VI

Random vs structured WSN:

Localization, Hierarchy, organization, Stationary vs. mobile, Energy efficient routing, sleeping modes, issues in WSNs.

Books Recommended

1. D.P. Agrawal and Qing-An zeng, “Introduction to Wireless and Mobile Systems” Thomson Learning
2. Martyn Mallick, Mobile and Wireless Design Essentials, Wiley, 2003
3. Kavesh Pahlavan and Prashant Krishnamurty - “Principles of Wireless Networks – A Unified Approach, Pearson Education, 2002

**I Year – II Sem. M.Tech.(DSCE)
MIMO OFDM Systems
(PROGRAM ELECTIVE-3)**

Code: 7U209

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Course Objectives:

This course is intended to impart to the students the principles of

- The fundamental concepts and design principles in “Multiple-Input Multiple-Output” (MIMO) wireless communications –channel capacity, antenna diversity, space-time coding.
- The fundamental concepts in “Orthogonal Frequency-Division Multiplexing” (OFDM) communications – transmission, synchronization, peak-to-average power ratio (PAPR) reduction.
- These fundamental concepts of massive MIMO will present a comprehensive analytical development of the various concepts in massive MIMO and mmWave MIMO technologies for 5G together with practical insights and problem solving.

Course Outcome:

After Learning this course, the student will be able to gain knowledge and understanding of:-

- Principles of wireless communication
- OFDM System Model
- Bit Error Rate Analysis
- MIMO System Model & MIMO Receivers
- MIMO Capacity, space-time coding
- Massive MIMO and mmWave MIMO technologies for 5G

UNIT 1: Principles of Wireless Communication: The wireless communication environment, modeling of wireless systems, System model for narrowband signals, Rayleigh fading wireless channel.

UNIT 2: OFDM: Introduction to OFDM System Model - Multicarrier Modulation and Cyclic Prefix- OFDM Issues of PAPR- Frequency and Timing Offset Issues.

UNIT 3: Bit Error Rate Analysis: BER performance of wireless systems, multiple receive antenna system model, BER in multi antenna wireless systems, Maximum ratio combining.

UNIT 4: Introduction to MIMO: MIMO system model, MIMO Zero Forcing Receiver, MIMO MMSE receiver, SVD of the MIMO Channel.

UNIT 5: Space Time Codes: Alamouti & Space Time Codes, Alamouti code, another OSTBC example, Non linear MIMO receiver (V-BLAST).

UNIT 6: Introduction to 5G Wireless Technologies: Overview of 5G wireless networks, Challenges for existing cellular networks, 5G key specs, mm-wave wireless communication, massive MIMO Technology, NOMA.

Text Books:

1. Principles of Modern Wireless Communication Systems Theory & Practice, Aditya K Jagannatham, McGraw Hills Publications.
2. Wireless Communications: Principles and Practice, Rappaport, Pearson Publications
3. Fundamentals of 5G mobile networks, Jonathan Rodriguez, Willey Publication

References:

1. OFDM for Wireless Communications Systems Ramjee Prasad, Artech House Publishers (2004).
2. MIMO Wireless Communications EzioBiglieri Robert Calderbank Anthony Constantinides Andrea Goldsmith Arogyaswami Paulraj H. Vincent Cambridge University Press (2007)
3. MIMO-OFDM for LTE, WiFi and WiMAX Li Wang, Ming Jiang, Lajos L. Hanzo, YosefAkhtman Weily 2011.

**I Year – II Sem. M.Tech.(DSCE)
DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES
(PROGRAM ELECTIVE-3)**

Code: 7U210

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After completing the course students are able to understand

1. Analyse DSP tools such as DFT, FFT and systems such as LTI, LTV using MATLAB.
2. Obtain and understand the dynamic range, precision, conversion errors and computational errors
3. Learn basic architectural features and building blocks of Digital signal processor.
4. Understand and apply Execution control like hardware looping, interrupts and pipelining etc., analyze the processor TMS320C54XX processor.
5. Implement various DSP algorithms on TMS320C54XX.
6. Interface Memory and I/O peripherals to programmable DSP devices.

Unit I

INTRODUCTION TO DIGITAL SIGNAL PROCESING

Introduction, A Digital signal-processing system, The sampling process, Discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation, Analysis and Design tool for DSP Systems MATLAB, DSP using MATLAB.

Unit II

COMPUTATIONAL ACCURACY IN DSP IMPLEMENTATIONS

Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

Unit III

ARCHITECTURES FOR PROGRAMMABLE DSP DEVICES

Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External interfacing.

Unit IV

EXECUTION CONTROL AND PIPELINING

Hardware looping, Interrupts, Stacks, Relative Branch support, Pipelining and Performance, Pipeline Depth, Interlocking, Branching effects, Interrupt effects, Pipeline Programming models.

PROGRAMMABLE DIGITAL SIGNAL PROCESSORS

Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX processors, Pipeline Operation of TMS320C54XX Processors.

Unit V

IMPLEMENTATIONS OF BASIC DSP ALGORITHMS

The Q-notation, FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, PID Controller, Adaptive Filters, 2-D Signal Processing.

IMPLEMENTATION OF FFT ALGORITHMS

An FFT Algorithm for DFT Computation, A Butterfly Computation, Overflow and scaling, Bit-Reversed index generation, An 8-Point FFT implementation on the TMS320C54XX, Computation of the signal spectrum.

Unit VI

INTERFACING MEMORY AND I/O PERIPHERALS TO PROGRAMMABLE DSP DEVICES

Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).

A Multichannel buffered serial port (McBSP), McBSP Programming, a CODEC interface circuit, CODEC programming, A CODEC-DSP interface example.

TEXT BOOKS

1. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.
2. DSP Processor Fundamentals, Architectures & Features – Lapsley et al. S. Chand & Co, 2000.

REFERENCES

1. Digital Signal Processors, Architecture, Programming and Applications – B. Venkata Ramani and M. Bhaskar, TMH, 2002.
2. Digital Signal Processing – Jonatham Stein, John Wiley, 2005.

**I Year – II Sem. M.Tech.(DSCE)
INTERNET OF THINGS
(PROGRAM ELECTIVE-3)**

Code: 7U215

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Course Objectives: The student will learn about

1. Terminology, technology and applications of IoT
2. IoT system management using M2M (machine to machine) with necessary protocols
3. Python Scripting Language preferred for many IoT applications
4. Raspberry PI as a hardware platform for IoT sensor interfacing
5. Implementation of web based services for IoT with case studies

Course Outcomes: After completing this course, student shall be able to

1. Identify the implementation layers of an IoT application system
2. Describe the management of an IoT system using necessary protocols
3. Design, Develop and Illustrate IoT applications using Raspberry PI platform and Python Scripting
4. Implement web based services on IoT devices

Unit I: Introduction to Internet of Things

Definition and Characteristics of IoT, Physical Design of IoT – IoT Protocols, IoT communication models, Iot Communication APIs IoT enabled Technologies – Wireless Sensor Networks, Cloud Computing, Big data analytics, Communication protocols, Embedded Systems, IoT Levels and Templates

Domain Specific IoTs – Home, City, Environment, Energy, Retail, Logistics, Agriculture, Industry, health and Lifestyle

Unit II: IoT and M2M

Software defined networks, network function virtualization, difference between SDN and NFV for IoT Basics; IoT System Management with NETCOZF, YANG- NETCONF, YANG, SNMP NETOPEER

Unit III: Developing IoT

IoT Design Methodology - Introduction to Python - Language features of Python, Data types, data structures, Control of flow, functions, modules, packaging, file handling, data/time operations, classes, Exception handling Python packages - JSON, XML, HTTPLib, URLLib, SMTPLib

Unit IV: IoT Physical Devices and Endpoints

Introduction to Raspberry PI-Interfaces (serial, SPI, I2C) Programming – Python program with Raspberry PI with focus of interfacing external gadgets, controlling output, reading input from pins.

Unit V: IoT Physical Servers and Cloud Offerings

Introduction to Cloud Storage models and communication APIs Webservice – Web server for IoT, Cloud for IoT, Python web application framework Designing a RESTful web API

Unit VI: Case Studies Illustrating IoT Design

Home Automation – Smart Lighting, Home intrusion detection, *Cities* – Smart parking, *Environment* – Weather monitoring system, Weather reporting bot, Air pollution monitoring, Forest fire detection, *Agriculture* – Smart irrigation, *Productivity applications* – IoT printer

TEXT BOOKS:

1. Internet of Things - A Hands-on Approach, Arshdeep Bahga and Vijay Madisetti, Universities Press, 2015, ISBN: 9788173719547
2. Getting Started with Raspberry Pi, Matt Richardson & Shawn Wallace, O'Reilly (SPD), 2014, ISBN: 9789350239759

**I Year – II Sem. M.Tech.(DSCE)
SYSTEM-ON-CHIP ARCHITECTURE
(PROGRAM ELECTIVE-3)**

Code: 7U216

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After completing the course students are able to understand

1. Understanding the abstraction in the hardware design. Learning the processor design and trade offs
2. Learning the architecture of ARM processor, execution of instructions
3. Learning how to programme a RAM processor with Architecture
4. Understanding the Memory concepts.
5. Understanding the structural support for the System Management.
6. Understanding the concepts of Operating systems.

Unit I: Introduction to processor design: Abstraction in hardware design, MUO a simple processor, Processor design trade off, design for low power consumption.

Unit II: ARM Processor as System-on-Chip: Acorn RISC machine – Architecture inheritance – ARM programming model – ARM development tools – 3 and 5 stage pipeline ARM organization – ARM instruction execution and implementation – ARM coprocessor interface.

Unit III: ARM assembly language programming: ARM instruction types – data transfer, data processing and control flow instructions – ARM instruction set – Coprocessor instructions.

Architectural support for high level language: Data types – abstraction in software design – Expressions – Loops – Functions and Procedures – Conditional statements – use of memory.

Unit IV: Memory Hierarchy: Memory size and speed – on chip memory – caches – cache design - an example – memory management.

Unit V: Architectural support for System Management: Advanced microcontroller bus architecture – ARM memory interface – ARM reference peripheral specification – Hardware system prototyping tools – Armulator – Debug architecture.

Unit VI: Architectural support for Operating System: An introduction to Operating Systems – ARM system control coprocessor – CP15 protection unit registers – ARM protection unit – CP15 MMU registers – ARM MMU architecture – Synchronization – Context switching input and output.

TEXT BOOKS

1. ARM System on Chip Architecture, Steve Furber, 2nd ed. 2000, Addison Wesley Professional.
2. Design of System on a Chip: Devices and Components, Ricardo Reis, 1st ed. 2004, Springer.

REFERENCE BOOKS

1. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology), Jason Andrews, Newnes, BK and CDROM.
2. System on Chip Verification: Methodologies and Techniques, Prakash Rasnikar, Peter Paterson and Leena Singh. L, 2001, Kluwer Academic Publisher.

**I Year – II Sem. M.Tech.
CMOS ANALOG & MIXED SIGNAL DESIGN
(PROGRAM ELECTIVE-3)**

Code: 7U217

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After completing the course students are able to understand

1. *Understanding basic circuit connections, functionality and their objectives.
Learning the procedures involved in Current Mirror, matching in MOSFET mirrors. Voltage dividers, band gap voltage references, referenced Self-biasing.*
2. *Understanding the design and functioning of Amplifiers and Feedback Amplifiers and their stability.*
3. *Understanding the design and functioning of different types of Differential Amplifiers and their merits and demerits.*
4. *Understanding the design and functioning of Operational Amplifiers like basic CMOS Op-Amp, OTA.*
5. *Learning the Non-Linear & Dynamic Analog Circuits and their designing and Applications.*
6. *Learning the Data Converter Fundamentals, DAC & ADC specifications, Mixed Signal Layout issues, DAC architectures, ADC architectures*

A. CMOS ANALOG CIRCUITS:

Unit I

CURRENT SOURCES, SINKS & REFERENCES

The cascode connection, sensitivity and temperature analysis, transient response, layout of simple Current Mirror, matching in MOSFET mirrors, other Current Sources/Sinks.
Voltage dividers, current source self-biasing.

Unit II

AMPLIFIERS & FEEDBACK AMPLIFIERS

Gate Drain connected loads, Current Source Loads, Noise and Distortion, Class AB Amplifier.
Feedback Equation, properties of negative feedback and amplifier design, feedback topologies, amplifiers employing the four types of feedback, Stability.

Unit III

DIFFERENTIAL AMPLIFIERS

The Source Coupled pair, the Source Cross-Coupled pair, cascode loads, Wide-Swing Differential Amplifiers.

Unit IV

OPERATIONAL AMPLIFIERS

Basic CMOS Op-Amp Design, Operational Transconductance Amplifiers, Differential Output Op-Amp.

B. MIXED SIGNAL CIRCUITS:

Unit V

NON-LINEAR & DYNAMIC ANALOG CIRCUITS

Basic CMOS Comparator Design, Adaptive Biasing, Analog Multipliers, MOSFET Switch, Switched Capacitor circuits: Switched Capacitor Integrator, dynamic circuits.

Unit VI

DATA CONVERTER ARCHITECTURES

Data Converter Fundamentals, DAC & ADC specifications, Mixed Signal Layout issues, DAC architectures, ADC architectures.

TEXT BOOKS:

1. CMOS Circuit Design, Layout and Simulation - Baker, Li, Boyce, PHI, 2004.

REFERENCE BOOKS:

1. Analog Integrated Circuit Design - David A. Johns, Ken Martin, 1997, John Wiley & Sons
2. Design of Analog CMOS Circuits – B. Razavi, MGH, 2003, TMH.
 3. Analog MOS ICs for Signal Processing – R.Gregorian, Gabor C. Temes, John Wiley & Sons

**I Year – II Sem. M.Tech (DSCE)
EMBEDDED SYSTEMS LAB**

Code: 7U211

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After going through the Laboratory course, the student will be able to

1. Write the basic assembly language and Embedded C programs for timer, serial communication etc.
2. Interface various devices such as keyboard, ADC, DAC, LCD, Stepper Motor with 8051 microcontroller.
3. Study the Real Time Operating Systems and its applications.
4. Develop the device drivers for RT Linux.
5. Develop the Serial Communication drivers for ARM processor.
6. Design of RTOS kernel and study of Compile/Assembler.

Research Methodology:

Research Methodology: An Introduction; Defining the Research Problem; Overview of – (i) Research Design, (ii) Sampling Design, (iii) Measurement and Scaling Techniques, (iv) Methods of Data Collection, (v) Processing and Analysis of Data, (vi) Interpretation and Report Writing.

Text Books:

1. Research Methodology: Methods and Techniques, C.R. Kothari, 2nd ed. New Age International.
2. Research in Education, Best & Kahn, 9th ed. 2006, PHI

LIST OF EXPERIMENTS:

CYCLE 1 : 8051 MICROCONTROLLERS

Serial data Transmission using 8051 microcontroller in different modes

Look up tables for 8051

Timing subroutines for 8051 – Real time and applications

Keyboard interface to 8051

ADC, DAC interface to 8051

LCD interface to 8051

CYCLE 2 :

Study of Real Time Operating Systems

Development of Device Drivers for RT Linux

Software Development for DSP Applications

Serial Communication Drivers for ARM Processors

Case Studies : Any Two –

Design of RTOS Kernel

Cross Compiler / Assembler

Vx Works

**I Year – II Sem. M.Tech (DSCE)
Technical Seminar-2**

Code: 7U212

L T P C
- - 2 1

a	b	c	d	e	f	g	h	i	j	k
X	X	X	X	X	X			X		X

Max. Marks: 100

After studying this course, the students will be able to

1. Identify a research topic
2. Collect literature
3. Present seminar
4. Discuss the queries

There shall be three seminar presentations during I year I semester and I year II Semester. For seminar, a student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the Department in a report form and shall make an oral presentation before the Departmental Committee, which shall consist of the Head of the Department, a senior Faculty Member and the Supervisor and will jointly evaluate the report and presentation. For each Seminar there will be only internal evaluation of 25 marks. A candidate has to secure a minimum of 50% to be declared successful.

In the First semester the report must be in the form of the review paper with a format used by IEEE / ASME etc. In the Second semester Technical Seminar in the form of Independent Review Paper must be of high quality fit for publication in a reputed conference / journal.

The evaluation format for seminar is as follows:

- Day to day evaluation by the Supervisor : 20 marks
- Final Report : 20 marks
- Presentation : 60 marks (20 Abstract seminar +40 Final Presentation)

The presentation includes content (5) + Participation (5) + Presentation (10) for a total of 20 marks and double for 40 marks for final presentation.

A Student has to concentrate on the following sections while writing technical paper or presenting seminar.

Contents

- Identification of specific topic
- Analysis
- Organization of modules
- Naming Conventions
- Writing style
- Figures
- Feedback
- Miscellaneous

REFERENCES:

Teach Technical Writing in Two Hours per Week by Norman Ramsey

For Technical Seminar the student must learn few tips from sample seminars and correcting himself, which is continues learning process

REFERENCE LINKS:

5. <http://www.cs.dartmouth.edu/~scot/givingTalks/sld001.htm>

6. <http://www.cse.psu.edu/~yuanxie/advice.htm>

7. <http://www.eng.unt.edu/ian/guides/postscript/speaker.pdf>

NOTE: A student can use any references for this process, but must be shared in classroom.

**I Year – II Sem. M.Tech (DSCE)
COMPREHENSIVE VIVA VOCE**

Code: 7U213

								L	T	P	C
								-	-	2	1
a	b	c	d	e	f	g	h	i	j	k	
X	X	X	X	X	X			X		X	

Course Objective :

Evaluate, comprehend and assess of the concepts and the knowledge gained in the core courses of the first and the second year.

Course Outcomes :

At the end of this course, the student will be able to

1. Comprehend the concepts in the core and elective courses.
2. Exhibit technical knowlegde to face interviews.
3. Exhibit life long Learning skills for higher education and to persue Professional practice.

There will be 100 marks in total with 25 marks of internal evaluation and 75marks of external evaluation.

Internal:

Comprehensive Viva Voce is Conducted once in a semester and evaluated for 25 marks.

End examination : 75 Marks.

The end examination will be carried out by a committee consisting of an external examiner, head of the department, a senior faculty member and the supervisor. A candidate shall secure a minimum of 50% to be declared successful.

**I Year – II Sem. M.Tech.(DSCE)
MINI PROJECT WITH SEMINAR**

Code: 7U214

L	T	P	C
-	-	-	-

In I year II semester, a project seminar shall be conducted and (there is external evaluation). The evaluation for the project seminar shall be done in two stages, i.e. in the middle of the semester and at the end of the semester. The mid-semester seminar and the end semester the report for the mid-semester project seminar remaining marks shall be for presentation and discussion. The report for end semester project seminar and the remaining marks shall be for presentation and discussion. A candidate shall secure a minimum of 50% to be declared successful.

II Year – I Sem. M.Tech.(DSCE)
DESIGN OF FAULT TOLERANT SYSTEMS

Code: 7U301

L **T** **P** **C**
3 **-** **-** **3**

a	b	c	d	e	f	g	h	i	j	k
x	X		X	X				X		

After going through the course, the student will be able to

1. Demonstrate the concepts of reliability and other related terms and fault tolerance using different types of redundancy techniques.
2. Explore the concepts of fault checking circuits using totally self checking circuits, Berger code and residue codes.
3. Understand and explore the test pattern generation using ATPG process for stuck-at faults, transition delay and path delay faults.
4. Analyze various design for testability techniques such as Reed Muller’s expansion technique, OR-AND-OR design etc.
5. Understand the methods of sequential circuit testing using scan architecture and Boundary scan test.
6. Explore the various Built-in Self Test techniques for regular and irregular logic designs as well as for memory arrays.

Unit I

BASIC CONCEPTS: Reliability concepts, Failure & Faults, Reliability and failure rate, Relation between reliability and Mean-time between failure, Maintainability and Availability, Reliability of series, Parallel and Parallel-Series combinational circuits.

FAULT TOLERANT DESIGN: Basic concepts – Static, dynamic, hybrid, Triple Modular Redundant System, Self purging redundancy, Siftout redundancy (SMR), 5 MR re-configuration techniques, Use of error correcting code, Time redundancy and software redundancy.

Unit II

SELF CHECKING CIRCUITS: Basic concepts of Self checking circuits, Design of Totally Self Checking checker, Checkers using m out of n codes, Berger code, Low cost residue code.

FAIL SAFE DESIGN: Strongly fault secure circuits, fail safe design of sequential circuits using partition theory and Berger code, Totally self checking PLA design.

Unit III

Introduction to ATPG, ATPG process – Testability and Fault Analysis methods, Fault masking, Transition delay fault ATPG, Path delay, fault ATPG.

Unit IV

DESIGN FOR TESTABILITY FOR COMBINATIONAL CIRCUITS: Basic concepts of testability, controllability and observability, the Reed Muller’s expansion technique, OR-AND-OR design, use of control and syndrome testable designs.

Unit V

Scan Architectures and Techniques: Introduction to scan based testing, functional testing, the scan effective circuit, the MUX-D style scan flip-flops, the scan shift register, scan cell operation.

Scan Test Sequencing, scan test timing, partial scan, multiple scan chains, scan based design rules (LSSD), At-speed scan testing and architecture, multiple clock and scan domain operation, critical paths for At-speed scan test. Boundary Scan Test: JTAG Test Operations

Unit VI

BUILT IN SELF TEST (BIST): BIST concepts, Test pattern generation for BIST exhaustive testing, Pseudorandom testing, pseudo exhaustive testing, constant weight patterns, Generic offline BIST architecture, memory test architecture.

TEXT BOOKS:

1. Fault Tolerant & Fault Testable Hardware Design - Parag K. Lala, PHI
2. Design for Test for Digital ICs and Embedded Core Systems – Alfred L. Crouch, 2008, Pearson Education.
3. Fundamentals of Logic Design – Charles H. Roth, 5th ed., Cengage Learning.

REFERENCES:

1. Digital Systems Testing and Testable Design - M. Abramovili, M.A. Breues, A. D. Friedman, Jaico publications.
2. Essentials of Electronic Testing – Bushnell, and Vishwani D. Agarwal, Springers.

II Year – I Sem. M.Tech.(DSCE)
BANKING OPERATIONS, INSURANCE AND RISK MANAGEMENT
(OPEN ELECTIVE)

Code : 7ZC03

L **T** **P** **C**
3 **-** **-** **3**

a	b	c	d	e	f	g	h	i	j	k
							x			x

Course Objective: The objective of the course is to provide to students an understanding of Banking Operations, Insurance Market, and Risk Management Principles and techniques to control the risk, & the major Institutions involved and the Services offered within this framework.

UNIT I

INTRODUCTION TO BANKING BUSINESS: Introduction to Banking sectors-History of banking business in India, Structure of Indian banking system: Types of accounts, advances and deposits in a bank New Dimensions and products- E-Banking, Mobile-Banking, Net Banking, CRM, cheque system and KYC system.

UNIT II

BANKING REFORMS AND REGULATIONS: Banking regulation Act-1949, Reserve Bank of India Act-1934, Establishment of RBI, Functions and credit control system; Role of commercial banks and its functions. Banking sector reforms in India and deficiencies in Indian banking including problems accounts and Non-Performing Assets.

UNIT III

INTRODUCTION TO INSURANCE: Introduction to insurance, Need and importance of Insurance, principles of Insurance, characteristics of insurance contract, branches of insurance and types of insurance; life insurance and its products: Role of Agents and brokers.

UNIT IV

INSURANCE BUSINESS ENVIRONMENT: Regulatory and legal frame work governing the insurance sector, history of IRDA and its functions: Business and economics of insurance, need for changing mindset and latest trends.

UNIT V

INTRODUCTION TO RISK MANAGEMENT: Introduction to Risk, meaning and types of risk in business and individual, Risk management process, methods: Risk identification and measurement, Risk management techniques; Non insurance methods.

UNIT VI

FINANCIAL RISK MANAGEMENT: Introduction to Financial markets. Financial risk management techniques –Derivatives, Hedging and Portfolio management techniques: Derivatives and types of Derivatives-Futures, options and swaps: Shares, Commodity and Currency trading in India.

Books Recommended:

- Varshney, P.N., Banking Law and Practice, Sultan Chand & Sons, New Delhi.
- General Principles of Insurance Harding and Evariantly
- Mark S. Dorfman: Risk Management and Insurance, Pearson, 2009.
- Reddy K S and Rao R N: Banking and Insurance, Paramount publishers, 2013

References:

- Scott E. Harringam Gregory R. Nichanus: Risk Management & Insurance, TMH, 2009.
- Geroge E. Rejda: Principles of risk Management & Insurance, 9/e, pearson Education. 2009.
- G. Koteswar: Risk Management Insurance and Derivatives, Himalaya, 2008.
- Gulati: Principles of Insurance Management, Excel, 2009.
- James S Trieschmann, Robert E. Hoyt & David N. Sommer: Risk Mgt. & Insurance, Cengage, 2009.
- Dorfman: Introduction to Risk Management and Insurance, 8/e, Pearson, 2009.
- P.K. Gupta: Insurance and Risk Management, Himalaya, 2009.
- Vivek & P.N. Asthana: Financial Risk Management, Himalaya, 2009.
- Jyotsna Sethi & Nishwan Bhatia : Elements of Banking and Insurance, 2/e,PHI, 2012.

II Year – I Sem. M.Tech. (DSCE)
ENTREPRENEURSHIP AND INNOVATION
(OPEN ELECTIVE)

Code: 7ZC13

L **T** **P** **C**
3 **-** **-** **3**

a	b	c	d	e	f	g	h	i	j	k
X					X	X		X		X

Course Objective: The objective of the course is to make students understand the nature of entrepreneurship, and to motivate the student to start his/her own enterprise with innovative skills.

UNIT I

NATURE OF ENTREPRENEURSHIP: Characteristics, Qualities and skills of an Entrepreneur, functions of entrepreneur, Entrepreneur scenario in India and Abroad. Forms of Entrepreneurship: Small Business, Importance in Indian Economy, Types of ownership, sole trading, partnership, Joint Stock Company and other forms. First-Mover disadvantages, Risk Reduction strategies, Market scope strategy, Imitation strategies, and Managing Newness.

UNIT II

ASPECTS OF PROMOTION: Generation of new entry opportunity, SWOT Analysis, Technological Competitiveness, legal regulatory systems, patents and trademarks, Intellectual Property Rights- Project Planning and Feasibility Studies- Major steps in product development.

UNIT III

MANAGEMENT OF SMALL BUSINESS: Pre feasibility study - Ownership - budgeting – project profile preparation - Feasibility Report preparation - Evaluation Criteria- Market and channel selection- Product launching - Monitoring and Evaluation of Business- Effective Management of Small business.

UNIT IV

SUPPORT SYSTEMS FOR ENTREPRENEURS: Institutional Support, Training institution, Financial Institutions and Aspects: Sources of raising Capital, Debt-Equity, Financing by Commercial Banks, Government Grants and Subsidies, Entrepreneurship Promotion Schemes of Department of Industries (DIC), KVIC, SIDBI, NABARD, NSIC, APSFC, IFCI and IDBI. New Financial Instruments. Research and Development – Marketing and legal aspects, Taxation benefits, Global aspects of Entrepreneurship.

UNIT V

INTRODUCTION TO INNOVATION: Meaning of innovation, sources of innovative opportunity, 7 sources of innovative opportunity, Principles of innovation, the enablers of innovation, business insights, insights for innovation, technical architecture for innovation, focus on the essence of innovation.

UNIT VI

PROCESS AND STRATEGIES FOR INNOVATION: Process of innovation, the need for a conceptual approach, Factors contributing to successful technological innovation, Strategies that aim at innovation, impediments to value creation and innovation.

Books Recommended:

- Robert D Hisrich, Michael P Peters, Dean A Shepherd: Entrepreneurship, TMH, 2009
- Peter Drucker (1993), “Innovation and Entrepreneurship”, Hyper Business Book.

References:

- Bholanath Dutta: Entrepreneurship – Text and cases, Excel, 2009.
- Vasanth Desai: Entrepreneurship, HPH, 2009
- Barringer: Entrepreneurship, Pearson, 2009.
- C.K. Prahalad, M.S. Krishnan, The new age of Innovation – TATA McGRAW-HILL Edition 2008
- H. Nandan: Fundamentals of Entrepreneurship, PHI, 2009.
- Stay Hungry Stay Foolish, Rashmi Bansal and published by IIM., Ahmedabad

**II Year – I Sem. M.Tech.(DSCE)
NETWORK SECURITY AND CRYPTOGRAPHY
(OPEN ELECTIVE)**

Code : 7P307

L T P C
3 - - 3

a	b	c	d	e	f	g	h	i	j	k
X	X	X								

After completing the course students are able to understand

CO1:Students will be familiar with Different types of security attacks, security mechanisms, security services, conventional Encryption model and techniques

CO2:After completion of this unit students will be aware of modern encryption techniques

CO3: Students will get about the topics which are technological centric fundamentals of conventional cryptography principles and algorithms

CO4:After completion of this unit students can understand to know how the message is provided authentication using hash functions

CO5:Students will be familiar with Significance of Digital signature and authentication protocols

CO6:After reading this unit students will aware of about the topics of Internet Protocol security

UNIT-I

Introduction:

Attacks, Services and Mechanisms, Security attacks, Security services, A Model for Internetwork security. Classical Techniques: Conventional Encryption model, Steganography, Classical Encryption Techniques.

UNIT-II

Modern Techniques:

Simplified DES, Block Cipher Principles, Data Encryption standard, Strength of DES, Differential and Linear Cryptanalysis, Block Cipher Design Principles and Modes of operations.

Algorithms: Triple DES, International Data Encryption algorithm, Blowfish, RC5, CAST-128, RC2, Characteristics of Advanced Symmetric block ciphers.

UNIT-III

Conventional Encryption

Placement of Encryption function, Traffic confidentiality, Key distribution, Random Number Generation.

Public Key Cryptography

Principles, RSA Algorithm, Key Management, Diffie-Hellman Key exchange, Elliptic Curve Cryptography.

UNIT-IV

Number theory

Prime and Relatively prime numbers, Modular arithmetic, Fermat's and Euler's theorems, Testing for primality, Euclid's Algorithm, the Chinese remainder theorem, Discrete logarithms.

Message authentication and Hash functions:

Authentication requirements and functions, Message Authentication, Hash functions, Security of Hash functions and MACs.

UNIT-V

Hash and Mac Algorithms

MD File, Message digest Algorithm, Secure Hash Algorithm, RIPEMD-160, HMAC.

Digital signatures and Authentication protocols:

Digital signatures, Authentication Protocols, Digital signature standards.

Authentication Applications:

Kerberos, X.509 directory Authentication service. Electronic Mail Security: Pretty Good Privacy, S/MIME.

UNIT-VI**IP Security**

Overview, Architecture, Authentication, Encapsulating Security Payload, Combining security Associations, Key Management.

Web Security

Web Security requirements, Secure sockets layer and Transport layer security, Secure Electronic Transaction.

Intruders, Viruses and Worms : Intruders, Viruses and Related threats.

Fire Walls : Fire wall Design Principles, Trusted systems.

TEXT BOOKS:

1. Cryptography and Network Security: Principles and Practice - William Stallings, 2000, PE.

REFERENCES:

1. Principles of Network and Systems Administration, Mark Burgess, John Wiel

**II Year – I Sem. M.Tech.(DSCE)
Fundamentals of Renewable Energy Sources
(OPEN ELECTIVE)**

Code : 7X336

L T P C
3 - - 3

a	b	c	d	e	f	g	h	i	j	k
X	X	X								

OBJECTIVES:

At The End Of The Course, The Students Are Expected To Identify The New Methodologies / Technologies For Effective Utilization Of Renewable Energy Sources.

UNIT I : INTRODUCTION

World Energy Use – Reserves Of Energy Resources – Environmental Aspects Of Energy Utilisation – Renewable Energy Scenario In Tamil Nadu, India And Around The World – Potentials – Achievements / Applications – Economics Of Renewable Energy Systems.

UNIT II : SOLAR ENERGY

Solar Radiation – Measurements Of Solar Radiation – Flat Plate And Concentrating Collectors – Solar Direct Thermal Applications – Solar Thermal Power Generation – Fundamentals Of Solar Photo Voltaic Conversion – Solar Cells – Solar PV Power Generation – Solar PV Applications.

UNIT III : WIND ENERGY

Wind Data And Energy Estimation – Types Of Wind Energy Systems – Performance – Site Selection – Details Of Wind Turbine Generator – Safety And Environmental Aspects

UNIT IV : BIO – ENERGY

Biomass Direct Combustion – Biomass Gasifiers – Biogas Plants – Digesters – Ethanol Production – Bio Diesel – Cogeneration – Biomass Applications

UNIT V : OTHER RENEWABLE ENERGY SOURCES

Tidal Energy – Wave Energy – Open And Closed OTEC Cycles – Small Hydro-Geothermal Energy – Hydrogen And Storage – Fuel Cell Systems – Hybrid Systems.

OUTCOMES:

- Upon Completion Of This Course, The Students Can Able To Identify The New Methodologies / Technologies For Effective Utilization Of Renewable Energy Sources.

TEXT BOOKS:

- Rai. G.D., “Non Conventional Energy Sources”, Khanna Publishers, New Delhi, 2011.
- Twidell, J.W. & Weir, A., “Renewable Energy Sources”, EFN Spon Ltd., UK, 2006.

REFERENCES:

- Sukhatme. S.P., “Solar Energy”, Tata McGraw Hill Publishing Company Ltd., New Delhi, 1997.
- Godfrey Boyle, “Renewable Energy, Power For A Sustainable Future”, Oxford University Press, U.K., 1996.
- Tiwari. G.N., Solar Energy – “Fundamentals Design, Modelling & Applications”, Narosa Publishing House, New Delhi, 2002.
- Freris. L.L., “Wind Energy Conversion Systems”, Prentice Hall, UK, 1990.
- Johnson Gary, L. “Wind Energy Systems”, Prentice Hall, New York, 1985
- David M. Mousdale – “Introduction To Biofuels”, CRC Press, Taylor & Francis Group, USA 2010
- Chetan Singh Solanki, Solar Photovoltaics, “Fundamentals, Technologies And Applications”, PHI Learning Private Limited, New Delhi, 2009.

II Year – I Sem. M.Tech.(DSCE)
BUSINESS ANALYTICS
(OPEN ELECTIVE)

Code : 7ZC31

L	T	P	C
3	-	-	3

UNIT I

BUSINESS INTELLIGENCE: Business Intelligence – Definition and importance in organizations, Evolution of BI , BI at all levels in organization, Future of BI. Components of BI, BI applications.

UNIT II

BUSINESS ANALYTICS: Business Analytics – Definition and importance, Business analytics Process, Relationship between BA and Organization decision making process, BA's at strategic level to gain competitive advantage ,an overview of BA models.

UNIT III

DATA WAREHOUSE: Definition of DW, Importance and goals of DW, DW Architecture, and Online Analytical Processing: Concepts of OLTP and OLAP, multidimensional analysis - MOLAP, ROLAP

UNIT IV

DATA MINING: Introduction to Data Mining: Concept, KDD process, benefits of data mining, steps in data mining, data mining for business problems. Data Mining Tasks-Trend analysis, cluster analysis, text mining, web mining...etc.

UNIT V

DECISION MODELS: Descriptive, Predictive, Prescriptive Introduction to R software - Introduction and importance in analytical environment ,costs and benefits using R ,R in BA, Data mining ,Business Dashboards and reporting and few examples..

UNIT VI

BIG DATA: Concept of big data, significance, business applications of big data, introduction to Apache Hadoop, business performance management - performance measurement, metrics, KPIs and Business Activity Monitoring (BAM).

Books Recommended

- Prasad, R. N., &Seema Acharya, "Fundamentals of Business Analytics", Wiley India, New Delhi, 2014
- Gert H. N. Laursen, Jesper Thorlund, Business Analytics for Managers: Taking Business Intelligence Beyond Reporting, Wiley

Essential Recommended:

- Peter C. Bell, Gregory S. Zaric , Analytics for Managers: With Excel,Routledge
- Ohry,R for Business Analytics ,Springer

II Year – I Sem. M.Tech.(DSCE)
COST MANAGEMENT OF ENGINEERING PROJECTS
(OPEN ELECTIVE)

Code : 7ZC32

L	T	P	C
3	-	-	3

Course objective: To provide the insights of various project management and cost control techniques for successful implementation and completion of the project.

UNIT I

INTRODUCTION AND OVERVIEW OF THE STRATEGIC COST MANAGEMENT

PROCESS: Cost concepts in decision-making; Relevant cost, Differential cost, Incremental cost and Opportunity cost. Objectives of a Costing System; Inventory valuation; Creation of a Database for operational control; Provision of data for Decision-Making.

UNIT II

COST BEHAVIOR AND PROFIT PLANNING MARGINAL COSTING; Distinction between Marginal Costing and Absorption Costing; Break-even Analysis, Cost-Volume-Profit Analysis. Various decision-making problems. Standard Costing and Variance Analysis (Theory). Pricing strategies: Pareto Analysis. Target costing, Life Cycle Costing. Costing of service sector.

UNIT III

BUDGETARY CONTROL: Flexible Budgets; Performance budgets; Zero-based budgets. Measurement of Divisional profitability pricing decisions including transfer pricing

UNIT IV

PROJECT MANAGEMENT TECHNIQUES: Material Requirement Planning, Enterprise Resource Planning, Total Quality Management and Theory of constraints. Activity-Based Cost Management, Bench Marking; Balanced Score Card and Value-Chain Analysis.

UNIT V

PROJECT EVALUATION:. Meaning of Project, Detailed Engineering activities. Pre project execution main clearances and documents Project team : Role of Project Manager. Importance Project site. Project execution Project cost control. Bar charts and Network diagram.

UNIT VI

QUANTITATIVE TECHNIQUES: For cost management, Linear Programming, PERT/CPM, Transportation problems, Assignment problems, Simulation, Learning Curve Theory.

Books Recommended:

- Cost Accounting A Managerial Emphasis, Prentice Hall of India, New Delhi
- Charles T. Horngren and George Foster, Advanced Management Accounting

References:

- Robert S Kaplan Anthony A. Alkinson, Management & Cost Accounting
- Ashish K. Bhattacharya, Principles & Practices of CostAccounting A. H. Wheeler publisher
- N.D. Vohra, Quantitative Techniques in Management, Tata McGraw Hill Book Co. Ltd.

II Year – I Sem. M.Tech.(DSCE)
MINI PROJECT WITH SEMINARS

Code: 7U302

L	T	P	C
-	-	6	3

In II year I semester, a project work review shall be done by Internal and External for 100 marks and for 3 credits (there is external evaluation) in the semester. The evaluation for the project reviews shall be done in 2 stages (not less than 4 weeks between two consecutive stages) each stage internal marks 25 and average of two internal marks end semester evaluation.

External examiner project review marks and the end semester review shall carry 75 marks (50% by PRC and 50% by supervisor). The Supervisor and PRC will examine the Problem Definition, Objectives, Scope of Work, Literature Survey and design in Project Review- I. A candidate shall secure a minimum of 50% to be declared successful in Project Review- I. If candidate fails to fulfill minimum marks, he has to reappear during the supplementary examination.

II Year – I Sem. M.Tech.(DSCE)
MAIN PROJECT PHASE-1 with SEMINAR

Code: 7U303

L **T** **P** **C**
- **-** **10** **5**

A	b	c	d	e	f	g	h	i	j	k
X	X	X	X	X	X	X	X	X	X	X

Every candidate is required to submit thesis or dissertation after taking up a topic approved by the Project Review Committee.

A Project Review Committee (PRC) shall be constituted comprising of Heads of all the Departments which are offering the M.Tech programs and three other senior faculty members concerned with the M.Tech. programme.

Registration of Project Work: A candidate is permitted to register for the project work after satisfying the attendance requirement of all the previous semesters and after obtaining the approval of the PRC.

A candidate has to submit, in consultation with his project supervisor, the title, objective and plan of action of his project work to the PRC for its approval. Only after obtaining the approval of PRC the student can initiate the Project work. This process is to be completed within four weeks of commencement of II year I semester.

The student shall submit a project report at the end of II year I semester, and the same shall be evaluated at the end of that semester by the PRC. In the case of Unsatisfactory declaration, the student shall re-submit the Project report after carrying out the necessary modifications / additions in the Project work, within the specified time as suggested by the PRC.

**II Year – II Sem. M.Tech.(DSCE)
MAIN PROJECT PHASE-2 with SEMINAR**

Code: 7U401

L T P C
- - 12 6

a	b	c	d	e	f	g	h	i	j	k
X	X	X	X				X	X		X

In II year II semester, a project work review shall be done by PRC for 25 marks and for 6 credits (there is external evaluation) in the semester. The evaluation for the project reviews shall be done in 2stages (not less than 4 weeks between two consecutive stages) each stage internal marks 25 and average of two internal marks including end semester evaluation.

External examiner project review and the end semester review shall carry 75 marks (50% by PRC and 50% by supervisor). In the case of Project Review II, the Supervisor and PRC will examine implementation, testing and final execution of the project. A candidate shall secure a minimum of 50% to be declared successful in Project review II. If candidate fails to fulfill minimum marks, he has to reappear during the supplementary examination

**II Year – II Sem. M.Tech (DSCE)
DISSERTATION AND DEFENSE VIVA**

Code: 7U402

L T P C
- - - 7

a	b	c	d	e	f	g	h	i	j	k
X	X	X	X	X	X	X	X	X	X	X

Course Outcome: By the end of this course, students will be able to

1. Critically and theoretically analyze the systems/products they are going to design or develop.
2. Apply the theoretical knowledge gained to bring out innovative products.
3. Effectively communicate in a variety of forms including written, visual, verbal, online and technical literacy.
4. Work and participate as effective members in a group within a professional environment.
5. Develop an ongoing critical awareness of learning needs in the application of appropriate technologies.
6. Gain as much knowledge and experience in areas of the area of Digital Systems and Computer Electronics

EVALUATION OF PROJECT/DISSERTATION WORK

Every candidate shall be required to submit a thesis or dissertation on a topic approved by the Project Review Committee.

1. A Project Review Committee (PRC) shall be constituted with Head of the Department as Chairperson, Project Supervisor and one senior faculty member of the Departments offering the M. Tech. Programme.
2. Registration of Project Work: A candidate is permitted to register for the project work after satisfying the attendance requirement of all the subjects, both theory and practical.
3. After satisfying 2, a candidate has to submit, in consultation with his Project Supervisor, the title, objective and plan of action of his project work to the PRC for approval. Only after obtaining the approval of the PRC the student can initiate the Project work.
4. If a candidate wishes to change his supervisor or topic of the project, he can do so with the approval of the PRC. However, the PRC shall examine whether or not the change of topic/supervisor leads to a major change of his initial plans of project proposal. If yes, his date of registration for the project work starts from the date of change of Supervisor or topic as the case may be.
5. A candidate shall submit his project status report in four stages at least with a gap of 4 weeks between two consecutive stages.
6. The work on the project shall be initiated at the beginning of the II year and the duration of the project is two semesters. A candidate is permitted to submit Project Thesis only after successful completion of all theory and practical courses (no backlogs) with the approval of PRC not earlier than 40 weeks from the date of registration of the project work. For the approval of PRC the candidate shall submit the draft copy of thesis to the Head of the Department and make an oral presentation before the PRC.
7. After approval from the PRC, the soft copy of the thesis should be submitted to the College for ANTI-PLAGIARISM for the quality check and the plagiarism report should be included in the final thesis. If the copied information is less than 24%, then only thesis will be accepted for submission.
- 8 Three copies of the Project Thesis certified by the supervisor shall be submitted to the College.
- 9 In II year I semester and II semester, a project work review I and II shall be done by PRC for 100 marks and for 12 credits (there is no external evaluation) in each of the semester. The evaluation for the project reviews shall be done in 4 stages (not less than 4 weeks between two consecutive stages) including end semester evaluation. Each stage project review shall carry 20 marks and the end semester review shall carry 40 marks (50% by PRC and 50% by supervisor). The Supervisor and PRC will examine the Problem Definition, Objectives, Scope of Work,

Literature Survey and design in Project Review I. In the case of Project Review II, the Supervisor and PRC will examine implementation, testing and final execution of the project. A candidate shall secure a minimum of 50% to be declared successful in Project review I and II. If candidate fails to fulfill minimum marks, he has to reappear during the supplementary examination.

10. For Project Evaluation (Viva Voce) in II Year II Sem. there are external marks of 150 for 7 credits. HoD shall submit a panel of 3 examiners, eminent in that field. Principal will appoint one of them as examiner.

11. The thesis shall be adjudicated by examiner selected by the College. If the report of the examiner is not favourable, the candidate shall revise and resubmit the Thesis. If the report of the examiner is unfavourable again, the thesis shall be summarily rejected.

12. If the report of the examiner is favourable, Project Viva-Voce examination shall be conducted by a board consisting of the Supervisor, Head of the Department and the external examiner who adjudicated the Thesis. Candidate has to secure minimum of 50% marks in Project Evaluation (Viva-Voce) examination.

13. If he fails to fulfill as specified in 12, he will reappear for the Viva-Voce examination only after three months. In the reappeared examination also, fails to fulfill, he will not be eligible for the award of the degree.

14. The Head of the Department shall coordinate and make arrangements for the conduct of Project Viva- Voce examination.