COURSE STRUCTURE
AND
DETAILED SYLLABUS
for

M.Tech course

in

DIGITAL SYSTEMS & COMPUTER ELECTRONICS

(ECE)

(Applicable for the batches admitted from 2017-2018)

Department of Electronics and Communication Engineering (ECE)

SREENIDHI INSTITUTE OF SCIENCE AND TECHNOLOGY

(An Autonomous Institution approved by UGC and affiliated to JNTUH)

(Accredited by NAAC with 'A' Grade, Accredited by NBA of AICTE, Recipient of WBA under TEQIP I & II)

Yamnampet, Ghatkesar, Malkagiri(Medchal)-501 301.

M.Tech. (Digital Systems & Computer Electronics)
Course Structure and Syllabus
Academic Regulations: 2017-18

I YEAR - I Semester

Sl. No.	Code	Subject	L	T	P	Credits	Internal marks	External marks
1.	6U101	Digital System Design	3	1	-	3	25	75
2.	6U102	Advanced Data Communications	3	1	-	3	25	75
3.	6U103	Advanced Microprocessors and Microcontrollers	3	1	-	3	25	75
4.	6T101	VLSI Technology and Design	3	1	-	3	25	75
5.		Elective-I	3	1	-	3	25	75
6.		Elective-II	3	1	-	3	25	75
7.	6U104	Research Methodology	2	-	-	2	25	75
8.	6U171	VLSI Technology and Design Lab	-	-	4	2	25	75
9.	6U172	Literature Review Seminar -1	-	-	3	1	100	-
10.	6U173	Comprehensive Viva-Voce-1	-	-	-	1	50	50
		Total	**20**	**6**	**7**	**24**	**350**	**650**

I YEAR - II Semester

Sl. No.	Code	Subject	L	T	P	Credits	Internal marks	External Marks
1.	6U201	Advanced Computer Architecture	3	1	-	3	25	75
2.	6T204	Low Power VLSI Design	3	1	-	3	25	75
3.	6U202	Design of Fault Tolerant Systems	3	1	-	3	25	75
4.	6T202	Embedded Real Time Operating Systems	3	1	-	3	25	75
5.		Open Elective	3	1	-	3	25	75
6.		Elective-III	3	1	-	3	25	75
7.	6U271	Embedded Systems Lab	-	-	4	2	25	75
8.	6U272	Literature Review Seminar -2	-	-	3	1	100	-
9.	6U273	Project Seminar-1(Abstract)	-	-	3	2	100	-
10.	6U274	Comprehensive Viva-Voce-2	-	-	-	1	50	50
		Total	**18**	**6**	**10**	**24**	**425**	**575**

M.Tech. (Digital Systems & Computer Electronics)
Course Structure and Syllabus
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II YEAR – I Semester

Sl. No.	Code	Subject	L	T	P	Credits	Internal Marks	External Marks
1.	6U371	Project Seminar-2 (Design and Development)	-	-	-	4	100	-
2.	6U372	Project Work (Part I) Project Status Report	-	-	-	20	Grading*	-
		Total	-	-	-	**24**	**100**	-

*****Grading – Excellent/ Good/ Satisfactory/ Unsatisfactory

II YEAR – II Semester

Sl. No.	Code	Subject	L	T	P	Credits	Internal Marks	External Marks
1.	6U471	Project Seminar-3 (Impementation/ Execution)	-	-	-	2	100	-
2.	6U472	Pre submission Seminar	-	-	-	2	100	-
3.	6U473	Project Work and Dissertation	-	-	-	20	-	Grading*
		Total	-	-	-	**24**	**200**	-

*****Grading – Excellent/ Good/ Satisfactory/ Unsatisfactory

ELECTIVE I

1) 6U105 - Advanced Digital Signal Processing
2) 6UC01 - Image & Video Processing
3) 6U106 - Advanced Computer Networks
4) 6T103 - Hardware Software Co-Design
5) 6T109 - Internet of Things

ELECTIVE II

1) 6T102 - CPLD & FPGA Architectures and Applications
2) 6U107 - Internetworking
3) 6U108 - Digital Control Systems
4) 6U109 - Embedded system Design
5) 6T106 - Hardware Description Languages and FPGA Based Design

OPEN ELECTIVE

1) 6ZC13 - Entrepreneurship and Innovation
2) 6ZC03 - Banking Operation, Insurance and Risk Management
3) 6H233 - Ethics, Morals, Gender sensitization and Yoga
4) 6ZC04 - Network security and cryptography

ELECTIVE III

1) 6T201 - System on Chip Architecture
2) 6U203 - CMOS Analog & Mixed Signal Design
3) 6U204 - Digital Signal Processors and Architectures
4) 6U205 - Device Modeling
5) 6U206 - Adhoc &Wireless Sensor Networks

I Year -I Sem M.Tech. (DSCE)
DIGITAL SYSTEM DESIGN

Code : 6U101

L	T	P	C
3	1	-	3

a	b	c	d	e
x		x		x

After studying this course, the students will be able to

1. Explore the implementation of digital circuits using Programmable Devices such as PLA, PAL, ROM and FPGAs.
2. Understand the representation and implementation of sequential circuit with State Machine Charts, explained with examples.
3. Explore the importance and design aspects of Design for Testability.
4. Demonstrate different test pattern generation techniques to detect faults in combination circuits.
5. Describe the various Techniques of fault diagnosis in sequential circuits.
6. Explore the concepts of PLA minimization and PLA Testing.

Unit-I: Designing with Programmable Logic Devices
Designing with Read only memories – Programmable Logic Arrays – Programmable Array logic – Sequential Programmable Logic Devices – Design with FPGA's– Using a One-hot state assignment,
State transition table- State assignment for FPGA's - Problem of Initial state assignment for One –Hot encoding - State Machine charts – Derivation of SM Charts – Realization of SM charts – Design Examples –Serial adder with Accumulator - Binary Multiplier – Dice Game controller – Binary Divider – Control logic for Sequence detector – Realization with Multiplexer – PLA – PAL.

Unit-II: Fault Modeling
Logic Fault model – Fault detection & Redundancy- Fault equivalence and fault location –Fault dominance – Single stuck at fault model – Multiple stuck at fault models –Bridging fault model
Fault diagnosis of combinational circuits by conventional methods – Path sensitization techniques, Boolean Difference method – Kohavi algorithm, Test Algorithms- D-Algorithm.

Unit-III: Test Pattern Generation
Random testing, Transition count testing, Exhaustive Testing and Pseudo Random Testing. Signature analysis and test bridging faults.

Unit-IV: Fault Diagnosis in Sequential Circuits
Circuit Test Approach, Transition Check Approach - State identification and fault detection experiment, Machine identification, Design of fault detection experiment.

Unit-V: PLA Minimization and Testing
PLA Minimization – PLA folding, Fault model in PLA, Test generation and Testable PLA Design.

Unit-VI: Minimization and Transformation of Sequential Machines
The Finite state Model – Capabilities and limitations of FSM – State equivalence and machine minimization – Simplification of incompletely specified machines. Fundamental mode model – Flow table – State reduction – Minimal closed covers – Races, Cycles and Hazards.

TEXT BOOKS:
1. Fundamentals of Logic Design – Charles H. Roth, 5th ed., Cengage Learning.
2. Digital Systems Testing and Testable Design – Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman- John Wiley & Sons Inc.
3. Switching and Finite Automata Theory – Z. Kohavi , 2nd ed., 2001, TMH
4. Logic Design Theory – N. N. Biswas, PHI

REFERENCES :
1. Digital Design – Morris Mano, M.D.Ciletti, 5Th Edition, PHI.
2. Digital Circuits and Logic Design –Samuel C. Lee, PHI

I Year -I Sem M.Tech.(DSCE)

ADVANCED DATA COMMUNICATIONS

Code: 6U102

L	T	P	C
3	1	-	3

a	b	c	d	e	f
X	X		X		

After studying this course, the students will be able to

1.Describe and determine the performance of different digital modulation techniques for digital data transmission over the channel.

2. Describe data communication system model and different networks for transmission of digital data with different transmission modes and rates.

3. Describes the different error detection and correction schemes for transmission of digital information over the channel.

4. Describes the functions of Data Link control and design formats of various Data Link Protocols.

5. Describes different switching and multiplexing techniques for transmission of digital data.

6.Describe and determine the performance of Random access, controlled access and channelization protocols.

Unit-I:

Digital Modulation: Introduction, Information Capacity Bits, Bit Rate, Baud, and M-ARY Coding, ASK, FSK, PSK, QAM, BPSK, QPSK, 8PSK, 16PSK, 8QAM, 16QAM, DPSK – Methods, Band Width Efficiency, Carrier Recovery, Clock Recovery.

Applications: Ethernet

Unit -II:

Basic Concepts of Data Communications, Interfaces and Modems: Data Communication- Components, Networks, Distributed Processing, Network Criteria- Applications, Protocols and Standards, Standards Organizations- Regulatory Agencies, Line Configuration- Point-to-point- Multipoint, Topology- Mesh- Star- Tree- Bus- Ring- Hybrid Topologies, Transmission Modes- Simplex- Half duplex- Full Duplex, Categories of Networks- LAN, MAN, WAN and Internetworking, Digital Data Transmission- Parallel and Serial, DTE- DCE Interface- Data Terminal Equipment, Data Circuit- Terminating Equipment, Standards EIA 232 Interface, Other Interface Standards, Modems- Transmission Rates.

Unit-III:

Error Detection and Correction: Types of Errors- Single- Bit Error, CRC (Cyclic Redundancy Check)- Performance, Checksum, Error Correction- Single-Bit Error Correction, Hamming Code, convolution codes.

Unit-IV:

Data link Control: Stop and Wait, Sliding Window Protocols.

Data Link Protocols: Asynchronous Protocols, Synchronous Protocols, Character Oriented Protocol- Binary Synchronous Communication (BSC) - BSC Frames- Data Transparency, Bit Oriented Protocols – HDLC, Link Access Protocols. Byte oriented protocol-PPP

Unit-V:

Switching: Circuit Switching- Space Division Switches- Time Division Switches- TDM Bus- Space and Time Division Switching Combinations- Public Switched Telephone Network, Packet Switching- Datagram Approach- Virtual Circuit Approach- Circuit Switched Connection Versus Virtual Circuit Connection, Message Switching.

Multiplexing: Time Division Multiplexing (TDM), Synchronous Time Division Multiplexing, Digital Hierarchy, Statistical Time Division Multiplexing.

Unit-VI:

Multiple Access: Random Access, Aloha- Carrier Sense Multiple Access (CSMA)- Carrier Sense Multiple Access with Collision Detection (CSMA)- Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA), Controlled Access- Reservation- Polling- Token Passing, Channelization- Frequency- Division Multiple Access (FDMA), Time - Division Multiple Access (TDMA), - Code - Division Multiple Access (CDMA).

Applications: GSM and WCDMA.

TEXT BOOKS:

1. Data Communication and Computer Networking - B. A.Forouzan, 3rd ed., 2008, TMH.

2. Advanced Electronic Communication Systems - W. Tomasi, 5 ed., 2008, PEI.

REFERENCES:

1. Data Communications and Computer Networks - Prakash C. Gupta, 2006, PHI.

2. Data and Computer Communications - William Stallings, 8th ed., 2007, PHI.

3. Data Communication and Tele Processing Systems - T. Housely, 2nd Edition, 2008, BSP.

4. Data Communications and Computer Networks- Brijendra Singh, 2nd ed., 2005, PHI.

Telecommunication System Engineering – Roger L. Freeman, 4/ed., Wiley-Interscience, John Wiley & Sons, 2004.

I Year – I Sem. M.Tech. (DSCE)
ADVANCED MICROPROCESSORS AND MICROCONTROLLERS

Code: 6U103

L	T	P	C
3	1	-	3

a	b	c	d	e	f
X	X	X		X	X

After studying this course, the students will be able to

1. Understand the architecture, interfacing , instruction set and programming of 8086 microprocessor.
2. Understanding of high end Processors of X86 family,Multi-tasking and Multi-user Operating System.
3. Understanding the interfacing, interrupts, DMA, and working of cache memory, co-processors.
4. Undestanding basic architecture and development tools of ARM Processor.
5. Understanding of assembly language programmed and High Level Language support provided by ARM Processor.
6. Understanding the applications of microprocessor, microcontrollers, and ARM Processor and features of some standard serial interfaces.

UNIT-I
8086 microprocessor family overview, 8086 Internal Architecture, memory interfacing constructing the machine codes for 8086, Introduction to programming the 8086, writing programes with Assembler, Assembly Language program development tools.

UNIT-II
The 80486 and Pentium processors – The Intel 80286 microprocessor, The Intel 80386 32-Bit microprocessor architecture, The Intel 80486 microprocessor and pentium processor architecture concept of multiuser / multitasking operating system.

UNIT-III
Interfacing to 8086 microprocessor, 8086 Interrupts and Interrupt applications, Digital Interfacing, Analog interfacing and Industrial Control, DMA, Cache Memory and co-processors.

UNIT-IV
Introduction to Broad COM Processor Architecture: Architecture of BCM 2837 Processor

UNIT-V
LINUX Building Porting-Raseberry PI, Programs on Sensors, ADC, Serial Communication.

UNIT-VI
Atmel AVR Micro Controllers: Architecture, Introduction to Aurdino, Working with Aurdino Simple Programs.

TEXT BOOKS:
1. Microprocessors and Interfacing by DOUGLAS V HALL, Revised Second Edition, McGraw-Hill
2. Design with PIC microcontroller by Jhon B Peatman. Pearson education

Web Link:
1. https://www.raspberrypi.org
2. www.avr-tutorials.com
3. www.atmel.com

REFERENCES:
1. Embedded System Design, Frank Vahid, Tony Givargis, John Wiley.
2. Microcontrollers, Raj Kamal, Pearson Education.
3. An Embedded Software Primer, David E. Simon, Pearson Education.

I Year – I Sem. M.Tech. (DSCE)
VLSI TECHNOLOGY & DESIGN

Code: 6T101

L	T	P	C
3	1	-	3

a	b	c	d	e	f
X	X	X			

After studying this course, the students will be able to

1. *Understand the fabrication processes and electrical properties of various MOSFET's, their advantages and disadvantages.*
2. *Able to draw the Layout diagrams and Stick diagrams for CMOS gates and Circuits etc. Also understand about the design rules required during drawing of Layout diagrams and Stick diagrams.*
3. *Understand about various alternative gate circuits and able to analyze delay and power dissipation in them.*
4. *Understand and analyse various delays and power consumption in the combinational circuits. Student also able to test various combinational gates and circuits for faults.*
5. *Understand the need of clocking disciplines required for proper operation of sequential systems and also able to analyse various delays and power consumption in the sequential circuits.*
6. *Understand the floor planning methods, power, clock distribution and off-chip connections of a chip.*

Unit – I:
REVIEW OF MICROELECTRONICS AND INTRODUCTION TO MOS TECHNOLOGY: MOS, CMOS, BiCMOS Technologies.
BASIC ELECTRICAL PROPERTIES OF MOS AND BICMOS CIRCUITS: I_{ds} versus V_{ds} relationships, MOS Transistor Threshold Voltage V_t, MOS Transistor Transconductance(g_m) and Output Conductance(g_{ds}), Pass Transistor, nMOS Inverter, Determination of pull-up to pull down ratio(Zpu/Zpd) for an nMOS inverter driven by another nMOS inverter, Determination of pull-up to pull down ratio(Zpu/Zpd) for an nMOS inverter driven through one or more pass transistors, Alternative forms of Pull-Up, The CMOS Inverter, Latch-up in CMOS circuits, Bi CMOS Inverter.

Unit – II:
MOS TRANSISTOR PARASITICS:MOS Transistor circuit model.
LAYOUT DESIGN AND RULES: MOS Layers, Stick diagrams, Layout diagrams, Design rules for wires (nMOS and CMOS), 'λ' based design rules, Transistor Design rules(nMOS, pMOS and CMOS), Vias, cut, Design rules for Contacts in NMOS ckts, Buried and butting contacts.

Unit – III:
LOGIC GATES: Static Complementary Gates-Gate structures, Logic levels, Delay and Transition time, Power consumption, The Speed-Power product, Driving large loads; Alternative Gate circuits-Pseudo nMOS logic, DCVS logic, Domino logic, Low power gates.
INTERCONNECTS: Estimation of Resistance, Capacitance and Inductance parasitics, Delay through Resistive interconnects-Lumped model, Lumped RC Tree model, Lumped RC ladder model, Distributed RC ladder model; Delay through Inductive interconnect-Transmission line model, Cross-talk between RC wires.

Unit – IV:
COMBINATIONAL LOGIC NETWORKS: Standard Cell Based Layout Design, Layout of Full Adder, Left edge algorithm, Combinational Network delay-Fanout delay, Path delay, delay due to false path, Transistor sizing, Cross-talk minimization, Power optimization, Combinational logic Testing-Gate Testing, Network testing.

Unit –V:
SEQUENTIAL SYSTEMS: Latches and Flip-Flops-Latch, Flip-Flop, Setup and Hold times, Dynamic Latch circuit, Multiplexed Dynamic Latch circuit, Recalculating Static latch circuit, Clocked inverter, D-Latch built from clocked inverters, SR Flip-Flop, D-Flip-Flop; Sequential systems and Clocking disciplines-Clocking rule1, rule2, One phase systems for FFs, Two phase systems for Latches, Advanced clocking Analysis; Sequential system Design-Designing of one bit counter, Designing of a 01 string recognizer, State assignment-Encoding a Shift register, How state codes affect delay, Power optimization, testing-LSSD.

Unit – VI:

HIGH DENSITY MEMORY ELEMENTS: Architecture of a high density memory system, ROM, Static RAM, Dual ported SRAM, One transistor Dynamic RAM, Three transistor dynamic RAM.

FLOOR PLANNING: Floor planning methods-Block placement and Channel definition, Wind mill structures, Global routing, switch box routing, Power distribution, Clock distribution.

OFF-CHIP CONNECTIONS: Packages, Power line inductance, I/O Architecture, Pad Design.

TEXT BOOKS:

1. Essentials of VLSI Circuits and Systems, K. Eshraghian, Douglas A.Pucknell, 2005, PHI.
2. Modern VLSI Design - Wayne Wolf, 3rd ed., 1997, Pearson Education.
3. Digital Integrated Circuits A Design Perspective – Jan M.Rabaey, Ananta Chandrakasan, Borivoje Nikolic, Pearson Education

REFERENCES:

1. Principles of CMOS VLSI Design A System Perspective – Neil H.E.Weste, K. Eshraghian, Addison-Wesley Publishing Company.
2. Introduction to VLSI Circuits and Systems – John Uyemura, John Willey & Sons, Inc
3. VLSI design techniques for Analog and Digital Circuits – Randall L.Geiger, Phillip E.Allen, Noel R.StraderMcGraw-Hill Company
4. Application Specific Integrated circuits – Sabastian Smith, Pearson Education.

I Year – I Sem. M.Tech. (DSCE)
ADVANCED DIGITAL SIGNAL PROCESSING
(ELECTIVE-I)

Code : 6U105

L	T	P	C
3	1	-	3

a	b	c	d	e	f
X	X	X			

After going through the course, the student will be able to

1. Compute DFT and perform Linear Filtering ,Frequency Analysis of Signals using DFT.
2. Compute the Fast Fourier using the radix, Goertzel and Chrip-z Transform Algorithms.
3. Design IIR Filters using Butterworth and Chebyshev Approximations, and realise Structures for IIR Systems.
4. Design FIR Filters by several methods and realise Structures for FIR Systems
5. Define, represent, classify, analyse and also represent Multirate signal processing and its applications
6. Understand and predict both forward and backward linear predictors for optimum power estimation.

Unit I
DISCRETE FOURIER TRANSFORMS: Frequency domain Sampling, Properties of DFT, Linear Filtering Methods based on the DFT,Frequency Analysis of Signals using DFT.

Unit II
FAST FOURIER TRANSFORMS: Radix-2, Radix-4, Split Radix FFT Algorithms, The Goertzel Algorithm and Chrip-z Transform Algorithm.

Unit III
DESIGN OF IIR FILTERS: Design of IIR Filters using Butterworth and Chebyshev Approximations, Structures for IIR Systems –Direct Form, Cascade, Parallel, Lattice and Lattice-Ladder Structures.

Unit –IV
DESIGN OF FIR FILTERS: Fourier series method, Windowing Techniques, Design of Digital Filters based on Least-Squares Method, Structures for FIR Systems –Direct Form, Cascade, Lattice Structures.

Unit V
MULTIRATE SIGNAL PROCESSING: Introduction, Decimation by a factor D, Interpolation by a factor I, Sampling rate conversion by a rational factor I/D, Filter design & Implementation for sampling rate conversion.

Unit VI
Linear Prediction : Forward and Backward Linear Prediction – Forward Linear Prediction, Backward Linear Prediction, Optimum reflection coefficients for the Lattice Forward and Backward Predictors. Solution of the Normal Equations: Levinson Durbin Algorithm, Schur Algorithm. Properties of Linear Prediction Filters

TEXT BOOKS

1. Digital Signal Processing: Principles, Algorithms and Applications - J.G.Proakis & D.G.Manolokis, 5Th ed., PHI.
2. Discrete Time signal processing - Alan V Oppenheim & Ronald W Schaffer, PHI.
3. DSP – A Practical Approach – Emmanuel C.Ifeacher, Barrie. W. Jervis, 2nd ed., Pearson Education.

REFERENCE BOOKS

1. Digital Spectral Analysis with applications– S. Lawrence Marple Jr, Prentice-Hall Series in Signal Processing.
2. Modern spectral Estimation : Theory & Application – S. M .Kay, 1988, PHI.
3. Multirate Systems and Filter Banks – P.P.Vaidyanathan – Pearson Education
4. Digital Signal Processing – S.Salivahanan, A.Vallavaraj, C.Gnanapriya, 2000,TMH

I Year -I Sem M.Tech.(DSCE)
IMAGE & VIDEO PROCESSING
(ELECTIVE – I)

Code : 6UC01

L	T	P	C
3	1	-	3

a	b	c	d	e	f
X	X	X			X

After studying this course, the students will be able to

1. *Get the knowledge of the basic step in image processing system, Discrete cosine transforms and discrete wave let transforms.*
2. *Differentiate image enhancement methods ,different types of spatial domain and frequency domain methods.*
3. *Get the knowledge of point, line and edge detection, thresholding , Region based segmentation.*
4. *Differentiate different types of redundancies, lossy and lossy less image compression, different types of coding techniques.*
5. *Know the difference between analog video and digital video, different types of image formation and sampling of video signals*
6. *Study the different types of motion estimation techniques and application of motion estimation in video coding.*

Unit I: Fundamentals of Image Processing and Image Transforms

Basic steps of Image Processing System Sampling and Quantization of an image – Basic relationship between pixels
Image Transforms: 2 D- Discrete Fourier Transform, Discrete Cosine Transform (DCT), Wavelet Transforms: Continuous Wavelet Transform, Discrete Wavelet Transforms.

Unit II: Image Enhancement

Spatial domain methods: Histogram processing, Fundamentals of Spatial filtering, Smoothing spatial filters, Sharpening spatial filters.
Frequency domain methods: Basics of filtering in frequency domain, image smoothing, image sharpening, Selective filtering.

Unit III: Image Segmentation & Compression

Image Segmentation concepts, Point, Line and Edge Detection, Thresholding and Region Based segmentation. Image compression fundamentals - Coding Redundancy, Spatial and Temporal redundancy, Compression models: Lossy & Lossless, Huffman coding, Arithmetic coding, LZW coding, Run length coding, Bit plane coding, Transform coding, Predictive coding.

Unit IV: Basic steps of Video Processing

Analog Video, Digital Video. Time-Varying Image Formation models: Three-Dimensional Motion Models, Geometric Image Formation, Photometric Image Formation, Sampling of Video signals and filtering operations.

Unit V: 2-D Motion Estimation

Optical flow, General Methodologies, Pixel Based Motion Estimation, Block- Matching Algorithm, Mesh based Motion Estimation, Global Motion Estimation, Application of motion estimation in Video coding.

Unit VI: Three dimensional Motion Estimation & Waveform based coding

Feature based motion estimation, Direct Motion Estimation. **Block based transform coding**: over view, one dimensional unitary transform, two dimensional unitary transform, The discrete cosine transform, Bit allocation

and transform coding gain , **Predictive Coding:** over view, optimal predictor design and predictive coding gain, Block based hybrid video coding.

TEXT BOOKS

1. Digital Image Processing – Gonzaleze and Woods, 3rd ed., Pearson.
2. Video processing and communication – Yao Wang, Joem Ostermann and Ya–quin Zhang. 1st Ed., PH Int.

REFERENCE BOOKS

1. Digital Video Processing – M. Tekalp, Prentice Hall International

I Year – I Sem. M.Tech.(DSCE)
ADVANCED COMPUTER NETWORKS
(ELECTIVE – I)

Code: 6U106

L	T	P	C
3	1	-	3

a	b	c	d	e	f
x	x	x			

After completing the course students are able to

1. *Get the knowledge of congestion control Quality of Service and queue management.*
2. *Describes Wireless LAN topologies, and its requirements, the design issues and functions of physical layer, Medium access control (MAC) layer.*
3. *Describes Wireless Personal Area Networks , first generation to third generation Cellular systems, protocols and architecture of IEEE 802.16 standard and Wireless ATM.*
4. *Describes Cellular Systems and Infrastructure, Virtual Private network*
5. *Describes ATM Protocol Reference model ,ATM Traffic and Service Parameterization.*
6. *Describes Interconnection Networks and SONET architecture*

Unit – I

Congestion and Quality of Service (QoS): Data traffic congestion, congestion control, open loop and closed loop congestion control in TCP and Frame Relay, Quality of Service, Flow characterization, Flow classes, Need for QOS, Resource allocation, Best effort service features, Techniques to improve QoS.

Queue Management: Passive, active (RED), and Fair (BRED, choke) Queue management schemes, scheduling, traffic shaping, Resource reservation and Admission Control Scheduling, Integrated and Differential services.

Unit – II

Wireless Local Area Network: Introduction, Wireless LAN topologies, Wireless LAN requirements, the Physical layer, Medium access control (MAC) layer, Latest Developments.

Unit – III

Wireless Personal Area Networks (WPANs): Introduction to PAN technology and applications, Commercial alternatives – Bluetooth, Home RF.

Wireless Wide Area Networks and MANs: The cellular concept, Cellular architecture, First Generation Cellular systems, Second Generation Cellular systems, Third Generation Cellular systems, Wireless in Local Loop, Wireless ATM, IEEE 802.16 standard.

Unit – IV

Cellular Systems and Infrastructure – Based Wireless Networks: Cellular Systems Fundamentals, Channel Reuse, SIR and User Capacity, Interference reduction techniques, Dynamic resource allocation, Fundamental rate limits.

Virtual Private network (VPN): Types of VPN, VPN General Architecture, Current VPN advantages and disadvantages, VPN security issues, VPN standards.

Unit – V

ATM Protocol Reference Model: Introduction, Transmision Convergence (TC) sub-layer, Physical Medium Dependent (PMD) sub-layer, Physical layer standards for ATM.

ATM Layer: ATM Cell structure Header at UNI, ATM Cell structure Header at NNI, ATM Layer functions.

ATM Adaptation Layer: Service classes and ATM Adaptation layer, ATM Adaptation Layer 1 (AAL1), ATM Adaptation Layer 2 (AAL2), ATM Adaptation Layer 3/4 (AAL3/4), ATM Adaptation Layer 5 (AAL5).

ATM Traffic and Service Parameterization: ATM traffic parameters, ATM service parameters, Factors affecting QoS parameters, ATM service categories, QoS and QoS Classes.

Unit – VI: Interconnection Networks: Introduction, Banyan Networks – Properties, Crossbar switch, Three stage class networks, Rearrangeable networks, Folding algorithm, Benes networks, Looping algorithm, Bit-Allocation Algorithm.
SONET/SDH: SONET/SDH Architecture, SONET Layers, SONET Frames, STS Multiplexing, SONET Networks.

TEXT BOOKS:

1. Wireless Communications – Andrea Goldsmith, 2005, Cambridge University Press.
2. Ad Hoc Wireless Networks: Architectures and Protocols – C. Siva Ram Murthy and B.S. Manoj, 2004, PHI.
3. Data Communication and Networking - B.A. Forouzan, 2004, TMH.

REFERENCES:

1. Introduction to Broadband Communication Systems– Sadiku, Mathew N.O., Akujuobi, Cajetan M., PHI
2. Wireless Networks – P. Nicopolitidis, A.S. Pomportsis, G.I. Papadimitriou, M.S. Obaidat, 2003, John Wiley & Sons.
3. High Performance TCP / IP Networking – Mahaboob Hassan, Jain Raj, PHI.

I Year – I Sem. M.Tech.(DSCE)
HARDWARE- SOFTWARE CO-DESIGN
(ELECTIVE-I)

Code: 6T103

L	T	P	C
3	1	-	3

a	b	c	d	e
X	X	X		

After going through the course, the student will be able to

1: Able to understand models, architecture, methodology and languages for co-design. Hardware-Software algorithms are studied
2: To understand Prototyping and emulation techniques, environments, future developments, architecture Specialization techniques and system communication infrastructure
3: Study of target architectures
4: Study of compilation technologies and tools for embedded processor architectures
5: Able to understand computational model, interfacing components, design and implementation verification, verification tools
6: Study of design representation for system level synthesis, system level specification languages

Unit –I
CO- DESIGN ISSUES
Co- Design Models, Architectures, Languages, a Generic Co-design Methodology.

CO- SYNTHESIS ALGORITHMS
Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

Unit –II
PROTOTYPING AND EMULATION
Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

Unit -III
TARGET ARCHITECTURES
Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

Unit – IV
COMPILATION TECHNIQUES AND TOOLS FOR EMBEDDED PROCESSOR ARCHITECTURES
Modern embedded architectures, embedded software development needs, compilation technologies practical consideration in a compiler development environment.

Unit – V
DESIGN SPECIFICATION AND VERIFICATION
Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

Unit – VI
LANGUAGES FOR SYSTEM – LEVEL SPECIFICATION AND DESIGN-I
System – level specification, design representation for system level synthesis, system level specification languages
LANGUAGES FOR SYSTEM – LEVEL SPECIFICATION AND DESIGN-II
Heterogeneous specifications and multi language co-simulation the cosyma system and lycos system.

TEXT BOOKS

1. Hardware / software co- design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – 2009, Springer.
2. Hardware / software co- design Principles and Practice, 2002, Kluwer Academic Publishers

I Year – I Sem. M.Tech.(DSCE)
INTERNET OF THINGS
(ELECTIVE-I)

Code: 6T107

L	T	P	C
3	1	-	3

a	b	c	d	e	f
x	x				

Course Objectives: The student will learn about

1. Terminology, technology and applications of IoT
2. IoT system management using M2M (machine to machine) with necessary protocols
3. Python Scripting Language preferred for many IoT applications
4. Raspberry PI as a hardware platform for IoT sensor interfacing
5. Implementation of web based services for IoT with case studies

Course Outcomes: After completing this course, student shall be able to

1. Identify the implementation layers of an IoT application system
2. Describe the management of an IoT system using necessary protocols
3. Design, Develop and Illustrate IoT applications using Raspberry PI platform and Python Scripting
4. Implement web based services on IoT devices

Unit I: Introduction to Internet of Things

Definition and Characteristics of IoT, Physical Design of IoT – IoT Protocols, IoT communication models, Iot Communication APIs IoT enabaled Technologies – Wireless Sensor Networks, Cloud Computing, Big data analytics, Communication protocols, Embedded Systems, IoT Levels and Templates
Domain Specific IoTs – Home, City, Environment, Energy, Retail, Logistics, Agriculture, Industry, health and Lifestyle

Unit II: IoT and M2M

Software defined networks, network function virtualization, difference between SDN and NFV for IoT Basics; IoT System Management with NETCOZF, YANG- NETCONF, YANG, SNMP NETOPEER

Unit III: Developing IoT

IoT Design Methodology - Introduction to Python - Language features of Python, Data types, data structures, Control of flow, functions, modules, packaging, file handling, data/time operations, classes, Exception handling Python packages - JSON, XML, HTTPLib, URLLib, SMTPLib

Unit IV: IoT Physical Devices and Endpoints

Introduction to Raspberry PI-Interfaces (serial, SPI, I2C) Programming – Python program with Raspberry PI with focus of interfacing external gadgets, controlling output, reading input from pins.

Unit V: IoT Physical Servers and Cloud Offerings
Introduction to Cloud Storage models and communication APIs Webserver – Web server for IoT, Cloud for IoT, Python web application framework Designing a RESTful web API

Unit VI: Case Studies Illustrating IoT Design
Home Automation – Smart Lighting, Home intrusion detection, ***Cities*** – Smart parking, ***Environment*** – Weather monitoring system, Weather reporting bot, Air pollution monitoring, Forest fire detection, ***Agriculture*** – Smart irrigation, ***Productivity applications*** – IoT printer

TEXT BOOKS:

1. Internet of Things - A Hands-on Approach, Arshdeep Bahga and Vijay Madisetti, Universities Press, 2015, ISBN: 9788173719547

2. Getting Started with Raspberry Pi, Matt Richardson & Shawn Wallace, O'Reilly (SPD), 2014, ISBN: 9789350239759

I Year – I Sem. M.Tech. (Digital Systems & Computer Electronics)
CPLD & FPGA ARCHITECTURES AND APPLICATIONS
(Elective II)

Code:6T102

L	T	P	C
3	1	-	3

a	b	c	d	e	f
X	X	X		X	

After studying this course, the students will be able to

1. *Understand the classification of PLDs and Architectures of AMD and Altera Flex-10K series CPLD.*
2. *Understand the basic architecture of Spartan-3 FPGA architecture, Artix-7 series FPGA*
3. *Understand the basic design flow of FPGA using EDA Tools: Xilinx ISE project navigator, Xilinx Vivado System Design.*
4. *Design the Combinational logic designs with various examples.*
5. *Design the Sequential logic designs with various examples. Understand and explore the FSM and FSMD designs of digital systems using available EDA tools.*
6. *Understand and analyze the front-end designs and case studies of digital system designs using EDA tools.*

Unit –I
Programmable logic : Classification of PLDs, Features, architectures of complex programmable logic devices, AMD, Altera FLEX logic-10000 series CPLD.

Unit –II
FPGA Architectures: Overview of a general FPGA device, Xilinx FPGA versions and specifications, Xilinx Spartan-3 FPGA architecture, Artix-7 series FPGA architectural features and specifications. Speed performance and in system programmability.

Unit – III

DESIGN FLOW OF FPGA AND EDA SOFTWARE: Development flow: RTL code, testbench, RTL simulation, synthesis, implementation, static timing analysis, device programming, Overview of FPGA Design flow.

Unit-IV
RTL DIGITAL DESIGNS-1: Combinational circuit designs, routing structure of conditional control constructs, implementation of if- statement and parallel case statement for priority routing network, general coding guidelines for an always block, common errors in combinational circuit codes, parameter and constant. Design example: Hexadecimal digit to seven segment LED decoder, barrel shifter, floating point adder, ALU design.

Unit-V
RTL DIGITAL DESIGNS-II: Sequential designs: HDL for D-FF, register, shift register, universal shifter, synchronous and asynchronous counter designs.
FSM and FSMD: FSM representation, state diagram, ASM chart, Moore based designs, Mealy based designs, single RT operation, ASMD Chart and its code development, binary to BCD conversion, division circuit.

Unit - VI
Digital front-end design tools for FPGAs & ASICs. Various EDA tools – Design flow using FPGAs. Method to incorporate memory modules, HDL examples for Single and dual port RAM, ROM.

TEXT BOOKS:

1. FPGA PROTOTYPING BY VERILOG EXAMPLES –Pong P. Chu, WILEY Publications.
2. FPGA based System Design- W. Wolf, Prentice Hall, 2004.
3. Embedded Core Design with FPGAs-Zainalabedin Navabi, Tata McGraw-Hill Publications.

REFERENCES:

1. Digital Design Using Field Programmable Gate Array, P.K.Chan & S. Mourad, 1994, Prentice Hall.
2. Data sheets of Artix 7 series FPGA from Xilinx website.
3. User guide of Xilinx Vivado System Design from Xilinx Website.
4. Digital Systems Design with FPGA's and CPLDs – Ian Grout, 2009, Elsevier.

I Year -I Sem M.Tech. (DSCE)
INTERNETWORKING
(ELECTIVE – II)

Code: 6U107

L	T	P	C
3	1	-	3

a	b	c	d	e	f
X	X	X			

After studying this course, the students will be able to

1.Describe Internet working concepts, IP Address and protocols
2.Understand the basic principle and operation of Internet Protocol and Transmission Control Protocol (TCP)
3. Understand the concepts of Stream Control Transmission Protocol, Mobile IP, Classical TCP Improvements.
4.Describe and determine the performance of Unicast and Multicast Routing Protocols.
5.Describe Domain Name System (DNS), TELNET protocols, SNMP and HTTP Architecture.
6.Describes basic principles of Multimedia, compression techniques, security mechanisms, protocols and Voice Over IP.

Unit -I:
Internetworking concepts: Principles of Internetworking, Connectionless Internetworking, Application level Interconnections, Network level Interconnection, Properties of the Internet, Internet Architecture, Wired LANS, Wireless LANs, Point-to-Point WANs, Switched WANs, Connecting Devices, TCP/IP Protocol Suite.

IP Address: Classful Addressing: Introduction, Classful Addressing, Other Issues, Sub-netting and Super-netting
IP Address: Classless Addressing: - Variable length Blocks, Sub-netting, Address Allocation. Delivery, Forwarding, and Routing of IP Packets: Delivery, Forwarding, Routing, Structure of Router.
ARP and RARP: ARP, ARP Package, RARP.

Unit -II:
Internet Protocol (IP): Datagram, Fragmentation, Options, Checksum, IP V.6.
Transmission Control Protocol (TCP): TCP Services, TCP Features, Segment, A TCP Connection, State Transition Diagram, Flow Control, Error Control, Congestion Control, TCP Times.

Unit -III:
Stream Control Transmission Protocol (SCTP): SCTP Services, SCTP Features, Packet Format, Flow Control, Error Control, Congestion Control.
Mobile IP: Addressing, Agents, Three Phases, Inefficiency in Mobile IP.
Classical TCP Improvements: Indirect TCP, Snooping TCP, Mobile TCP, Fast Retransmit/ Fast Recovery, Transmission/ Time Out Freezing, Selective Retransmission, Transaction Oriented TCP.

Unit -IV:
Unicast Routing Protocols (RIP, OSPF, and BGP: Intra and Inter-domain Routing, Distance Vector Routing, RIP, Link State Routing, OSPF, Path Vector Routing, BGP.
Multicasting and Multicast Routing Protocols: Unicast - Multicast- Broadcast, Multicast Applications, Multicast Routing, Multicast Link State Routing: MOSPF, Multicast Distance Vector: DVMRP.

Unit -V:
Domain Name System (DNS): Name Space, Domain Name Space, Distribution of Name Space, and DNS in the internet.
Remote Login TELNET:- Concept, Network Virtual Terminal (NVT). *File Transfer FTP and TFTP:* File Transfer Protocol (FTP). *Electronic Mail:* SMTP and POP.
Network Management-SNMP*:* Concept, Management Components. World Wide Web- HTTP Architecture.

Unit-VI:

Multimedia: Digitizing Audio and Video, Network security, security in the internet firewalls. Audio and Video Compression, Streaming Stored Audio/Video, Streaming Live Audio/Video, Real-Time Interactive Audio/Video, RTP, RTCP, Voice Over IP. Network Security, Security in the Internet, Firewalls.

TEXT BOOKS:

1. TCP/IP Protocol Suite- Behrouz A. Forouzan, Third Edition, TMH
2. Internetworking with TCP/IP Comer 3rd edition PHI

REFERENCES:

1. High performance TCP/IP Networking- Mahbub Hassan, Raj Jain, PHI, 2005
2. Data Communications & Networking – B.A. Forouzan – 2nd Edition – TMH
3. High Speed Networks and Internets- William Stallings, Pearson Education, 2002.
4. Data and Computer Communications, William Stallings, 7th Edition., PEI.

I Year – I Sem. M.Tech.(DSCE)
DIGITAL CONTROL SYSTEMS
(ELECTIVE – II)

Code: 6U108

	L	T	P	C
1.	3	1	-	3

a	b	c	d	e	f
X	X	X		X	

- Course Objectives:
  - ✓ To equip the students with the basic knowledge of A/D and D/A conversion and the basics of Z- Transform
  - ✓ To derive and analyze the transfer function multi-rate systems.
  - ✓ To evaluate the controllability, observability and stability of a system.
  - ✓ To equip the fundamental knowledge of time domain, Z-domain and frequency domain analysis.
  - ✓ To familiarize the concepts of discrete data control system.
- Course Outcomes:
  1. Students will have the basic knowledge of A/D and D/A conversion and analysis of discrete systems using Z-transform.
  2. Students will get the knowledge of deriving the system transfer function from block diagram and SFG.
  3. Students will explore various techniques for the analysis of controllability, observability and stability.
  4. Students will have the understanding of various techniques to analyze a system in time-domain and frequency domain.
  5. Students will have the knowledge of designing compensators and controllers for discrete data control systems.
  6. Students will have the knowledge to characterize MIMO systems.

2. Unit – I

3. Signal Conversion and Processing

Introduction, Digital Signals and Coding, Data conversion and Quantization, Sample and Hold devices, Analog to Digital conversion, Digital to Analog conversion, Mathematical modeling of the Sampling process, Sampling theorem, Mathematical modeling of Sampling by convolution integral, Flat Top approximation of the finite-pulse width sampling, Data construction and filtering of sampled signals, Zero order hold, first order hold, polygonal hold and slewer hold.

Review of Z–Transform and Applications: Review of Z–Transform, Applications of Z-Transform, Signals between sampling instants – submultiple sampling method & delayed Z-Transform and the Modified Z-Transform.

Unit – II

Transfer Functions, Block Diagrams and Signal Flow Graphs: Introduction, Pulse transfer function and Z-transfer function, Relation between G(s) and G(z), Closed loop systems, sampled signal flow graph, Modified Z-transfer function, Multirate discrete data systems (slow-fast, fast-slow, Multirate systems with all digital systems, Closed loop multi sampled systems, and cyclic rate sampled systems.

Unit – III

Controllability, Observability and Stability: Introduction, Controllability of Linear time invariant discrete data systems, Observability of Linear time invariant discrete data systems, Relationships between Controllability, Observability and Transfer Functions, Stability of Linear Digital Control Systems, Stability tests of discrete data systems (bilinear transformation method – Extension of RH criterion, Jurys stability test).

4.

5. Unit – IV

6. Time Domain and Z-Domain Analysis: Introduction, prototype second order system, comparison of time responses of continuous data abd discrete data systems, steay state error analysis of digital control systems, correlation between time response and root locations in S-plane and Z-plane, Dominant characteristic equation, Root loci of digital control systems, Effects of adding poles and zeroes to open loop transfer function.

7. Frequency Domain Analysis: Introduction, Polar plot of GH(z), Nyquist stability criterion, Bode plot,

Gain margin and Phase margin, Bandwidth considerations and Sensitivity analysis.

8. Unit-V
9. Design of Discrete Data Control Systems: Introduction, Cascade compensation by continuous data controllers, Design of continuous data controllers with equivalent digital controllers, Digital Controllers, Design of digital control systems with digital controllers and bilinear transformation.

Unit – VI

State Variable Technique: State equations of discrete data systems with sample and hold devices, State equations of digital systems with all digital elements, State transition equations (recursive method and Z-transform method), Relationship between State equations and Transfer Functions, Characteristic equation, Eigen values and Eigen vectors, Methods of computing the Transition Matrix (Cayley Hamilton theorem, Z-transform method), State diagrams of digital systems, De-composition of discrete data transfer functions.

TEXT BOOKS: 1. Digital Control Systems - Kuo, Oxford, 2nd Edition.

REFERENCES:

1. Discrete-Time Control Systems - Katsuhiko Ogata, 2nd Edition, PHI
2. Digital Control and State Variable Methods (Conventional and Intelligent Control Systems) by M.Gopal, 3rd edition, TMH

I Year – I Sem. M.Tech. (DSCE)
Embedded System Design
(ELECTIVE-II)

Code : 6T106

L	T	P	C
3	1	-	3

a	b	c	d	e	f
X	X	X			

On completion of this course you should be able to:

1. Understand the basic architecture of Embedded System and their classification.
2. Explore the architecture of ARM processor.
3. Understand the addressing modes and data processing instructions of ARM processor.
4. Understand the ARM thumb instruction set and its capabilities.
5. Use both assembly and C language based ARM programming.
6. Explore the memory management techniques in ARM.

UNIT-I

Introduction to embedded system:

Embedded system architecture, classifications of embedded systems, challenges and design issues in embedded systems, fundamentals of embedded processor and microcontrollers, CISC vs. RISC, fundamentals of Vonneuman/Harvard architectures, types of microcontrollers, selection of microcontrollers.

UNIT –II:

ARM Architecture:

ARM Design Philosophy, Registers, Program Status Register, Instruction Pipeline, Interrupts and Vector Table, Architecture Revision, ARM Processor Families.

UNIT –III:

ARM Programming Model – I:

Instruction Set: Data Processing Instructions, Addressing Modes, Branch, Load, Store Instructions, PSR Instructions, Conditional Instructions.

UNIT –IV:

ARM Programming Model – II:

Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instructions, Single-Register and Multi Register Load-Store Instructions, Stack, Software Interrupt Instructions

UNIT –V:

ARM Programming:

Simple C Programs using Function Calls, Pointers, Structures, Integer and Floating Point Arithmetic, Assembly Code using Instruction Scheduling, Register Allocation, Conditional Execution and Loops.

UNIT –VI:

Memory Management:

Cache Architecture, Polices, Flushing and Caches, MMU, Page Tables, Translation, Access Permissions, Context Switch.

TEXT BOOKS:

1. ARM Systems Developer's Guides- Designing & Optimizing System Software – Andrew N. Sloss, Dominic Symes, Chris Wright, 2008, Elsevier.

REFERENCE BOOKS:

Embedded Microcomputer Systems, Real Time Interfacing – Jonathan W. Valvano – Brookes / Cole, 1999, Thomas Learning.

I Year – I Sem. M.Tech.(DSCE)
HDL and FPGA based Design
(ELECTIVE-II)

Code : 6T109

L	T	P	C
3	1	-	3

a	b	c	d	e	f
X	X	X	X		x

After going through the course, the student will be able to

1. Understand the basics concepts of verilog.
2. Implementing digital designs using various types of modeling styles.
3. Understand the basic FPGA architecture and its programming.
4. Understand the FPGA design flow using EDA tools.
5. Understand the synthesis and implementation on FPGA using VHDL.
6. Understand the synthesis and implementation on FPGA using Verilog.

Unit-I

Verilog : basic concepts- Lexical conventions, data types, system tasks and compiler directives. Modules and ports. Gate level modeling- gate types, various types of gate delay specifications.

Unit-II

Data flow modeling- assignments, delays, expressions, operators, Behavioral modeling- structured procedures, procedural assignments, timing controls, conditional statements, loops, sequential and parallel blocks, generate blocks. Tasks and functions

Unit-III

FPGA Architectures and Technology. Historical background, channel type FPGA Xilinx Spartan 3E family, structured programmable array logic, programming FPGAs, benchmarking of FPGAs.

Unit-IV

Design Flow of FPGA and EDA Software: Development flow: RTL code, testbench, RTL simulation, synthesis, implementation, static timing analysis, device programming, Overview of Xilinx ISE project navigator, Xilinx Vivado System Design software flow.

Unit-V

VHDL Synthesis for FPGA Implementation.: Mapping of statements to gate assignment statements, logical, arithmetic and relational operators, vectors and slices, IF, Process, Case, Loop, Null, Wait statements. Modeling of flip-flops and latches. Modeling of FSM for synthesis. Some examples of synthesizable constructs.

Unit-VI

Verilog Synthesis for FPGA Implementation: Verilog constructs and operators, interpretation of Verilog constructs, synthesis design flow- RTL to gates, translation, un optimized intermediate representations, logic optimization, technology mapping and optimization, technology library, design constraints, optimized gate level description.

TEXT BOOKS:

1 S. Palnitkar, *Verilog HDL : A Guide to Digital Design and Synthesis*, PH/Pearson.
2 Pong P. Chu, FPGA Prototyping by Verilog Examples –WILEY Publications.
3. K. Coffman, *Real World FPGA Design with Verilog*, PH.

REFERENCES:

1. P.J. Ashenden, *The Designer's Guide to VHDL*, Second Edition, Morgan Kaufmann.
2. C. H. Roth, *Digital System Design with VHDL*, PWS/Brookscole.
3. R. C. Seals and G. F. Whapshott, *Programmable Logic : PLDs and FPGAs*, MH.
4. A,K. Sharma, *Programmable Logic Handbook : PLDs, CPLDs and FPGAs*, MH.

I Year – I Sem. M.Tech.(DSCE)
RESARCH METHODOLOGY

Code: 6U104

L	T	P	C
1	1	-	1

a	b	c	d	e	f
	X	X		X	X

After completing the course students are able to understand

1.Enumerate the concepts of Research, Characteristics and Prerequisites of research, Research needs in Engineering, Education, Science and Management .
2. Demonstrate the concepts of Conducting a literature search, Evaluating, Organizing, and synthesizing the literature.
3.Illustrate describing the research, finding the research Problem, Sources of research problem
4. Apprise Quantitative / Qualitative Research Design subjected to the situation of research
5. Contrast concept of formatting a research proposal.
6. Familiar with writing Research report.

Unit- I Overview on Research

What is Research? What is not Research? Meaning, aim, nature and scope of research, Characteristics and Prerequisites of research, Research needs in Engineering, Education, Science and Management, Research benefits to Society in general.

Unit II Literature Review
Role of Review, Search for related literature:On line search, Searching Web, -Conducting a literature search, Evaluating, Organizing, and synthesizing the literature.

Unit- III Research Intitation
Identifying and describing the research, Sources of research problem, Finding the research Problem, Criteria/ Characteristics of a Good research.

Unit – IV Data in Research, Research Methodlogy, and design tips of research
The Nature and role of Data in Research, Linking Data and Research Methodology, Validity of Method, Planning for Data collection.
Choosing a Research Approach, Establishing Research Criteria, Use of Quantitative / Qualitative Research Design, Feasibility of Research Design, Justification of Research Methodology.

Unit- V Research Proposal , treatment of data
Characteristics of a proposal, Formatting a research proposal, Preparation of proposal, Importance of Interpretation of data and treatment of data.

Unit- VI Research Report

Format of the Research report, Style of writing report, References and Bibliography.

REFERENCES

1. Paul D. Leedy and Jeanne E. Ormrod , "*Practical Research : planning and Design*", Printice Hall,(8th Edition),2004.
2. Ralph.J.Cecerone, "*On being scientist,"*,National academic press,3/e,2009.*(last article of UnitV)*
3. Sidhu K.S, " *Methodogy of Education Research*", Sterling Publishers Pvt Ltd (2009)
5. Kothari. C.R and gaurav garg, "*Research Methodology. Methods & Technique*", New age international publishers,2014.
6. A.K. S i n g h " Tests, Measurements and Research methods in Behavioural Sciences," Bharati Bhawan Publishers, 2015.

7. Gravetter and Forzano, "*Research methods for beaviour sciences,*"cenage publishers, 3/e,2012.
7. Y.P. Agarwal , "*Statistical Methods,*"Vantage press, 1986.
8. P.S Grewal , "Methods of Statistical Ananlysis,"Sterling Publishers,1990.
9. S.C. Gupta, V.K. Kapoor , "Fundamentals of Statistics,

I Year – I Sem. M.Tech.
VLSI Technology and Design LAB
(Common for DSCE and VLSI & Embedded Systems)

Code:6U171

L	T	P	C
-	-	4	2

a	b	c	d	e	f
X	X	X		X	X

After going through the Laboratory course, the student will be able to

1. *Design, Simulate, Verify, Synthesize Various Logic gates and also implement them on FPGA Board.*
2. *Design, Simulate, Synthesize and Implement various Combinational Logic Circuits and verify with FPGA Board.*
3. *Design, Simulate, Synthesize and Implement various Sequential Logic Circuits and verify with FPGA Board.*
4. *Schematic design and verification of logic Gates using Back end SW tool*
5. *Layout design, LVS verification, DC and AC analysis using Back end SW tool.*
6. *Schematic design and verification of OPAMP Circuits using Back end SW tool*

LIST OF EXPERIMENTS:

CYCLE 1: Combinational and Sequential Digital Circuit Design

Design the following experiments using Verilog HDL/VHDL, verify the RTL Design, perform Synthesis, Timing simulation, Implementation and verification on FPGA boards. Tools required: Front end SW tool and FPGA Boards.

1. Logic gates (Basic and Universal Gates)
2. Adders (HA, FA, Parallel Adders)
3. Decoders and Encoders
4. Multiplexers and Demultiplexers
5. Flip Flops (SR, D, JK, T)
6. Delay generation (1S, 2S etc.) and verification with LEDs
7. Seven Segment Display Interfacing
8. Synchronous Counter
9. Asynchrous Counter

CYCLE 2: VLSI Back End Design

Schematic design and verification, Layout design, LVS verification, DC and AC analysis of the following experiments. Tools required : Back end VLSI SW Tool.

1. Basic Gates (AND, OR & NOT)
2. Universal Gates (NOR / NAND)
3. Parity generators (even/odd)
4. Single stage OPAMP

I Year -I Sem M.Tech. (DSCE)
LITERATURE REVIEW SEMINAR - 1

Code: 6U172

L	T	P	C
-	-	3	1

Max. Marks: 100

a	b	c	d	e	f
X	X		X	x	

After Completing this course, the students will be able to

1. Identify a research topic
2. Collect literature
3. Present seminar
4. Discuss the queries

There shall be seminar presentations during I year I semester. Student shall collect the literature on a topic and critically review the literature and submit it to the Department in a report form,under the supervision of a faculty member and shall make an oral presentation before the Departmental Committee, which consists of the Head of the Department, a senior Faculty Member and the Supervisor , who will jointly evaluate the report and presentation. For each Seminar there will be only internal evaluation of 100 marks. A candidate has to secure a minimum of 50% to be declared successful.

In the First semester the report must be in the form of the review paper with a format used by IEEE / ASME etc. In the Second semester Technical Seminar in the form of Independent Review Paper must be of high quality fit for publication in a reputed conference / journal.

The evaluation format for seminar is as follows:

- Day to day evaluation by the Supervisor : 20 marks
- Final Report : 30 marks
- Presentation : 50 marks

A Student has to concentrate on the following sections while writing technical paper or presenting seminar.

Contents:

- Identification of specific topic
- Analysis
- Organization of modules
- Naming Conventions
- Writing style
- Figures
- Feedback
- Writing style
- Rejection
- Miscellaneous

REFERENCES:

Teach Technical Writing in Two Hours per Week by Norman Ramsey

For Technical Seminar the student must learn few tips from sample seminars and correcting himself, which is continues learning process

REFERENCE LINKS:

I. http://www.cs.dartmouth.edu/~scot/givingTalks/sld001.htm
II. http://www.cse.psu.edu/~yuanxie/advice.htm
III. http://www.eng.unt.edu/ian/guides/postscript/speaker.pdf

NOTE: A student can use any references for this process, but must be shared in classroom.

I Year – I Sem. M.Tech.(DSCE)
COMPREHENSIVE VIVA-VOCE -I

Code: 6U173

L	T	P	C
-	-	-	1

Max. Marks: 100

a	b	c	d	e	f
X			x	x	x

The Comprehensive Viva-Voce will be conducted by a Committee consisting of Head of the Department and two Senior Faculty members of the Department. The Comprehensive Viva-Voce is aimed to assess the students understanding in various subjects he/she studied during the M.Tech course of study. The Comprehensive Viva-Voce is valued for 100 marks by the Committee.

The internal marks for the Comprehensive Viva-Voce are 50 and external marks are 50 marks. A candidate has to secure a minimum of 50% to be declared successful

I Year – II Sem. M.Tech.(DSCE)
ADVANCED COMPUTER ARCHITECTURE

Code:6U201

L	T	P	C
3	1	-	3

a	b	c	d	e	f
X	X				

After studying this course, the students will be able to

1.Describe fundamentals of computer design instruction set and memory addressing .
2.Describe pipelines ,Pipeline hazards and RISC processor .
3.Describe cache memory and virtual memory.
4.Explain instruction level parallelism and dynamic scheduling
5. Explain multiprocessors and thread level parallelism
6.Describe practical issues in interconnecting networks and design of cluster

UNIT- I: Fundamentals of Computer Design
Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, quantitative principles of computer design, Amdahl's law.
Instruction set principles and examples- Introduction, classifying instruction set- memory addressing- type and size of operands, operations in the instruction set.

UNIT – II: Pipelines
Introduction ,basic RISC instruction set ,Simple implementation of RISC instruction set, Classic five stage pipe line for RISC processor, Basic performance issues in pipelining , Pipeline hazards, Reducing pipeline branch penalties.

UNIT - III
Memory Hierarchy Design
Introduction, review of ABC of cache, Cache performance , Reducing cache miss penalty, Virtual memory.

UNIT - IV Instruction Level Parallelism the Hardware Approach
Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, high performance instruction delivery- hardware based speculation.
ILP Software Approach
Basic compiler level techniques, static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues -Hardware verses Software.

UNIT –V: Multi Processors and Thread Level Parallelism
Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – memory architecture, Synchronization.

UNIT – VI: Inter Connection and Networks
Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters.
Intel Architecture
Intel IA- 64 ILP in embedded and mobile markets Fallacies and pit falls

TEXT BOOKS:
1. John L. Hennessy, David A. Patterson, Computer Architecture: A Quantitative Approach, 3rd Edition, An Imprint of Elsevier.

REFERENCE BOOKS:
1. John P. Shen and Miikko H. Lipasti, Modern Processor Design : Fundamentals of Super Scalar Processors
2. Computer Architecture and Parallel Processing ,Kai Hwang, Faye A.Brigs., MC Graw Hill.,
3. Advanced Computer Architecture - A Design Space Approach, Dezso Sima, Terence Fountain, Peter Kacsuk ,Pearson ed.

I Year – II Sem. M.Tech.(DSCE)
LOW POWER VLSI DESIGN

Code: 6T204

L	T	P	C
3	1	-	3

a	b	c	d	e	f
X	X	X	X		X

After going through the course, the student will be able to

1.Understand the implications of Low Power Design on IC Fabrication.
2.Understand the various deep submicron Processes and their future trends and directions.
3.Understand and analyse various MOSFET and Bipolar models and their limitations.
4.Know, Understand the conventional CMOS and BiCMOS logic gates, able to analyse power dissipation of the CMOS Inverter and its implementation of two- i/p NOR and NAND gates. He is also able to understand the basic driver configurations of the BiCMOS logic gate associated with shunting devices for full o/p voltage swing.
5. Understand the design of various low power BiCMOS circuits for high performance at low power supply voltages.
6.Trace out the reasons for Evolution of Latches and Flip flops. He is also able to understand the quality measures for latches and Flip flops and Design perspective.

Unit I
INTRODUCTION: low power design - an over view, **L**ow-Voltage, Low power design limitations, Silicon-on-Insulator Technology.

Unit II
MOS/BICMOS PROCESSES-TECHNOLOGY AND INTEGRATION: Introduction, The realization of BiCMOS processes-Low cost medium speed 5volts digital BiCMOS process, High performance high cost 5volts digital BiCMOS process, Twin well BiCMOS process; BiCMOS manufacturing and Integration considerations-Consideration for CMOS device structures, Process consideration for Bipolar transistors; Isolation in BiCMOS-Isolation in Bipolar transistors, Isolation in MOS transistors; Advanced isolation technologies.

Unit III

DEEP SUBMICRON PROCESSES: Polysilicon Emitter High-Performance BiCMOS Structure, Low capacitance Bipolar/BiCMOS Processes,SOI CMOS/BiCMOS VLSIs.
LOW-VOLTAGE/LOW POWER CMOS/ BICMOS PROCESSES: Low Voltage/Low Power SOI CMOS, Properties of fully depleted SOI MOSFETs, Low Voltage/Low Power Lateral BJT on SOI, Future trends and Directions of CMOS/BiCMOS processes.

Unit IV
CMOS AND Bi-CMOS LOGIC GATES: Conventional CMOS logic gates.
CONVENTIONAL BICMOS LOGIC GATES:Basic Driver configurations, Full swing with shunting devices, FS-CMBL, FS-CMBL with feedback, High performance CCBiCMOS circuit.

Unit V

LOW- VOLTAGE LOW POWER LOGIC CIRCUITS-1: BiCMOS Circuits Utilizing Lateral pnp BJTs in pMOS Structures, Merged BiCMOS Digital Circuits, Full-Swing Multi Drain/Multi Collector Complementary BiCMOS Buffers, Qasi Complementary BiCMOS Digital Circuits, Full-Swing BiCMOS/BiNMOS Digital Circuits Employing Schottky Diodes.

Unit VI

LOW- VOLTAGE LOW POWER LOGIC CIRCUITS-2: Feedback type BiCMOS Digital Circuits, High-Beta BiCMOS Digital Circuits, Transiently Saturated Full-Swing BiCMOS Digital Circuits, Bootstrapped-Type BiCMOS Digital Circuits-1.5volts Bootstrapped BiCMOS logic gate, Bootstrapped FS BiCMOS/BiNMOS Inverter, ESD-free Bi CMOS Digital Circuit.

TEXT BOOKS

1. CMOS/BiCMOS ULSI low voltage, low power by Yeo Rofail/ Gohl(3 Authors)-Pearson Education Asia 1st Indian reprint,2002

REFERENCES

1. Digital Integrated circuits , J.Rabaey PH. N.J 1996
2. CMOS Digital ICs , Sung-moKang and Yusuf Leblebici 3rd edition TMH 2003 (chapter 11)
3. VLSI DSP systems , Parhi, John Wiley & sons, 2003 (chapter 17)
4. IEEE Trans Electron Devices, IEEE J.Solid State Circuits, and other National and International Conferences and Symposia

I Year – II Sem. M.Tech.(DSCE)
DESIGN OF FAULT TOLERANT SYSTEMS

Code: 6U202

L	T	P	C
3	1	-	3

a	b	c	d	e	f
x	X	x		X	

After going through the course, the student will be able to

1. Demonstrate the concepts of reliability and other related terms and fault tolerance using different types of redundancy techniques.
2. Explore the concepts of fault checking circuits using totally self checking circuits, Berger code and residue codes.
3. Understand and explore the test pattern generation using ATPG process for stuck-at faults, transition delay and path delay faults.
4. Analyze various design for testability techniques such as Reed Muller's expansion technique, OR-AND-OR design etc.
5. Understand the methods of sequential circuit testing using scan architecture and Boundary scan test.
6. Explore the various Built-in Self Test techniques for regular and irregular logic designs as well as for memory arrays.

Unit I
BASIC CONCEPTS: Reliability concepts, Failure & Faults, Reliability and failure rate, Relation between reliability and Meantime between failure, Maintainability and Availability, Reliability of series, Parallel and Parallel-Series combinational circuits.
FAULT TOLERANT DESIGN: Basic concepts – Static, dynamic, hybrid, Triple Modular Redundant System, Self purging redundancy, Siftout redundancy (SMR), 5 MR re-configuration techniques, Use of error correcting code, Time redundancy and software redundancy.

Unit II
SELF CHECKING CIRCUITS: Basic concepts of Self checking circuits, Design of Totally Self Checking checker, Checkers using m out of n codes, Berger code, Low cost residue code.
FAIL SAFE DESIGN: Strongly fault secure circuits, fail safe design of sequential circuits using partition theory and Berger code, Totally self checking PLA design.

Unit III
Introduction to ATPG, ATPG process – Testability and Fault Analysis methods, Fault masking, Transition delay fault ATPG, Path delay, fault ATPG.

Unit IV
DESIGN FOR TESTABILITY FOR COMBINATIONAL CIRCUITS: Basic concepts of testability, controllability and observability, the Reed Muller's expansion technique, OR-AND-OR design, use of control and syndrome testable designs.

Unit V
Scan Architectures and Techniques: Introduction to scan based testing, functional testing, the scan effective circuit, the MUX-D style scan flip-flops, the scan shift register, scan cell operation.
Scan Test Sequencing, scan test timing, partial scan, multiple scan chains, scan based design rules (LSSD), At-speed scan testing and architecture, multiple clock and scan domain operation, critical paths for At-speed scan test. Boundary Scan Test: JTAG Test Operations

Unit VI
BUILT IN SELF TEST (BIST): BIST concepts, Test pattern generation for BIST exhaustive testing, Pseudorandom testing, pseudo exhaustive testing, constant weight patterns, Generic offline BIST architecture, memory test architecture.

TEXT BOOKS:

1. Fault Tolerant & Fault Testable Hardware Design - Parag K. Lala, PHI
2. Design for Test for Digital ICs and Embedded Core Systems – Alfred L. Crouch, 2008, Pearson Education.
3.Fundamentals of Logic Design – Charles H. Roth, 5th ed., Cengage Learning.

REFERENCES:

1. Digital Systems Testing and Testable Design - M. Abramovili, M.A. Breues, A. D. Friedman, Jaico publications.
2. Essentials of Electronic Testing – Bushnell, and Vishwani D. Agarwal, Springers.

I Year – II Sem. M.Tech.(DSCE)
EMBEDDED REAL TIME OPERATING SYSTEMS

Code: 6T202

L	T	P	C
3	1	-	3

a	b	c	d	e	f
X	X	X	X	X	X

After going through the course, the student will be able to

1: Understand embedded systems and various options and challenges in building them.
2. Understand the Real Time Systems and various parameters of tasks and models.
3. Understand various scheduling policies.
4. Understand the constructs used for inter-process communication.
5. Understand various services provided RTOS and Micro C/O.S.-II.
6.Understand Vx WORKS O.S. and some case studies

Unit I: Introduction
Embedded systems overview, design challenges, processor technology, I.C. technology, design technology, trade-offs. Single purpose processors, optimizing custom single purpose processors and general purpose processors, ASIPS, microcontrollers and DSP processors for embedded systems.

Unit II: Real Time Systems:
Typical real time applications, Hard Vs Soft real-time systems, A reference model of Real Time Systems: Processors and Resources, Temporal Parameters of real Time Work load, Periodic task model precedence constraints and data dependency, functional parameters, Resource Parameters of jobs and parameters of resources.

Unit III: Scheduling
Commonly used Approaches to Real Time Scheduling Clock Driven, Weighted Round Robin, Priority Driven, Dynamic Vs State Systems, Effective release time and Dead lines, Offline Vs Online Scheduling. Scheduling real time tasks in multi processor and distributed systems.

Unit IV: Inter-process Communication
Inter-process Communication and Synchronization of Processes, Tasks and Threads- Multiple Process in an Application, Problem of Sharing data by multiple tasks & routines, Inter-process communication

Unit V: Real Time Operating Systems & Programming Tools
Operating Systems Services, I/O Subsystems, RT & Embedded Systems OS, Interrupt Routine in RTOS Environment
Micro C/OS-II- Need of a well Tested & Debugged RTOs, Use of µCOS-II

Unit VI: VX Works & Case Studies
Memory managements task state transition diagram, pre-emptive priority, Scheduling context switches-semaphore- Binary mutex, counting watch dugs, I/O system
Case Studies of programming with RTOS- Case Study of Automatic Chocolate Vending m/c using µCOS RTOS, case study of sending application Layer byte Streams on a TCP/IP network, Case Study of an Embedded System for a smart card.

TEXT BOOKS:
1. Embedded Systems- Architecture, Programming and Design by Rajkamal, 2nd ed., 2008,TMH.
2. Real Time Systems- Jane W. S. Liu- PHI.
3. Real Time Systems- C.M.Krishna, KANG G. Shin, 1996, TMH
4.Embedded system Design-A unified hardware/ software approach by Frank Vahid, Tony D. Givargis, Johnwiley, 2002.

REFERENCES:
1. Advanced UNIX Programming, Richard Stevens
2. VX Works Programmers Guide

I Year – II Sem. M.Tech. (DSCE)
ENTERPRENEURSHIP AND INNOVATION
(OPEN ELECTIVE)

Code: 6ZC13

L	T	P	C
3	1	-	3

a	b	c	d	e	f
X		x	x	x	X

After studying this course, the students will be able to

1: Acquire qualities of an Entrepreneur
2: Understand how to set up an organization
3: Carry out SWOT analysis for setting up small business unit
4: Acquire decision making managerial behavior
5: Develop knowledge on getting financial support from various funding agencies
6: Buildup strategies for a successful business

The objective of the course is to make students understand the nature of entrepreneurship, and to motivate the student to start his/her own enterprise with innovative skills.

Unit 1: Nature of Entrepreneurship; Characteristics, Qualities and skills of an Entrepreneur, functions of entrepreneur, Entrepreneur scenario in India and Abroad. Forms of Entrepreneurship: Small Business, Importance in Indian Economy, Types of ownership, sole trading, partnership, Joint Stock Company and other forms. First-Mover disadvantages, Risk Reduction strategies, Market scope strategy, Imitation strategies, and Managing Newness.

Unit 2: Aspects of Promotion: Generation of new entry opportunity, SWOT Analysis, Technological Competitiveness, legal regulatory systems, patents and trademarks, Intellectual Property Rights- Project Planning and Feasibility Studies- Major steps in product development.

Unit 3: MANAGEMENT OF SMALL BUSINESS:
Pre feasibility study - Ownership - budgeting - project profile preparation - Feasibility Report preparation - Evaluation Criteria- Market and channel selection- Product launching - Monitoring and Evaluation of Business- Effective Management of Small business.

Unit 4: SUPPORT SYSTEMS FOR ENTREPRENEURS:
Institutional Support, Training institution, Financial Institutions and Aspects: Sources of raising Capital, Debt-Equity, Financing by Commercial Banks, Government Grants and Subsidies, Entrepreneurship Promotion Schemes of Department of Industries (DIC), KVIC, SIDBI, NABARD, NSIC, APSFC, IFCI and IDBI. New Financial Instruments. Research and Development – Marketing and legal aspects, Taxation benefits, Global aspects of Entrepreneurship.

Unit 5: INTRODUCTION TO INNOVATION:
Meaning of innovation, sources of innovative opportunity, 7 sources of innovative opportunity, Principles of innovation, the enablers of innovation, business insights, insights for innovation, technical architecture for innovation, focus on the essence of innovation.

Unit 6: PROCESS AND STRATEGIES FOR INNOVATION:
Process of innovation, the need for a conceptual approach, Factors contributing to successful technological innovation, Strategies that aim at innovation, impediments to value creation and innovation.

Text Books:

1. Robert D Hisrich, Michael P Peters, Dean A Shepherd: Entrepreneurship, TMH, 2009
2. H. Nandan: Fundamentals of Entrepreneurship, PHI, 2009.

References:

1. Bholanath Dutta: Entrepreneurship – Text and cases, Excel, 2009.
2. Vasanth Desai: Entrepreneurship, HPH, 2009
3. Barringer: Entrepreneurship, Pearson,2009.
4. Peter Drucker (1993), "Innovation and Entrepreneurship", Hyper Business Book.
5. C.K. Prahalad, M.S. Krishnan, The new age of Innovation – Tata McGraw-Hill,Edition 2008

I Year – II Sem. M.Tech.(VLSI & Embedded Systems)
BANKING OPERATIONS, INSURANCE AND RISK MANAGEMENT
(OPEN ELECTIVE)

Code : 6ZC03

L	T	P	C
3	1	-	3

a	b	c	d	e	f
			x		x

Course Objectives:

1) Describe the new dimensions and products served by the banking system in INDIA.
2) Explain the credit control system and create awareness on NPA's
3) Apply the knowledge of Insurance concepts in real life scenarios
4) Recognize the importance of regulatory and legal frame work of IRDA
5) Identify the risk management process and methods.
6) Calculate the diversity of risk and return

UNIT I

INTRODUCTION TO BANKING BUSINESS: Introduction to financial services - History of banking business in India, Structure of Indian banking system: Types of accounts, advances and deposits in a bank. KYC norms, New Dimensions and products- E-Banking: Mobile-Banking, Net Banking, Digital Banking, Negotiable Instruments: Cheque system.

UNIT II

BANKING SYSTEMS AND ITS REGULATION: Banking Systems: Branch Banking, Unit Banking, Correspondent Banking, Group Banking, Deposit Banking, Mixed Banking and Investment Banking - Banking Sector Reforms with special reference to Prudential Norms, Capital Adequacy Norms, Classification of Assets and NPA's, Functions of RBI, Role of RBI in regulating Indian Banking. Banking Ombudsman scheme.

UNIT III

INTRODUCTION TO INSURANCE: Introduction to insurance, Need and importance of Insurance, principles of Insurance, characteristics of insurance contract, branches of insurance and types of insurance: Life insurance and its products, General Insurance and its variants.

UNIT IV

INSURANCE BUSINESS ENVIRONMENT: Procedure for issuing an insurance policy –Nomination - Surrender Value - Policy Loans – Assignment - Revivals and Claim Settlement; Insurance as a tax mitigation tool, Role of IRDA in Insurance Regulation.

UNIT V

FINANCIAL MARKETS AND RISK MANAGEMENT: Introduction to Financial Markets: Money Market – Capital market; Introduction to Risk Management, meaning and classification of risks, Risk management process, Risk Management Approaches and Techniques.

UNIT VI

DERIVATIVES AS A RISK MANAGEMENT TOOL: Introduction to Financial Derivatives, Advantages of Derivatives - types of Derivative Contracts - Forwards, Futures, Options and Swaps - Differences among Forwards, Futures and Option Contracts.

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Books Recommended:

- Varshney, P.N., Banking Law and Practice, Sultan Chand & Sons, New Delhi.
- General Principles of Insurance Harding and Evantly
- Mark S. Dorfman: Risk Management and Insurance, Pearson, 2009.

References:

- Scott E. Harringam Gregory R. Nichanus: Risk Management & Insurance, TMH, 2009.
- Geroge E. Rejda: Principles of risk Management & Insurance, 9/e, pearson Education. 2009.
- G. Koteshwar: Risk Management Insurance and Derivatives, Himalaya, 2008.

I Year – II Sem. M.Tech.(DSCE)
GENDER SENSITIZATION, VALUES, ETHICS & YOGA
(OPEN ELECTIVE)

Code : 5ZC04

L	T	P	C
3	1	-	3

a	b	c	d	e	f
		x			x

Course Objective:

- To develop students' sensibility with regards to issues of gender in contemporary

  India and to help the students appreciate the essential complimentarity between 'VALUES and 'SKILLS' to ensure sustained happiness and prosperity which are the core aspirations of all human beings.
- To provide a critical perspective on the socialization of men, women and transgenders and to have a wider understanding of Ethics.
- To acknowledge women's role at home and at work.
- To help students reflect critically on gender violence, understand engineering ethics and an engineer's responsibility for safety and risk.
- Perceive gender literacy and understand the importance of gender perspective.
- Understand rules and principles set by the society in a customary way.
- Understand and appreciate the importance of personality development through yoga for a holistic life.

UNIT I: UNDERSTANDING GENDER AND VALUES
Importance of Gender sensitization, Gender Stereotyping
Socialization: Gender Socialization, Being modern in thought, yet rooted in one's culture
Just Relationships: Healthy relationship between men and women

UNIT II: GENDER SPECTRUM
Beyond the Binary, Gender Imbalance and its Consequences, Decline in Women population (Medico-legal concerns- PC and PNDT Act 1994), Social consequences of skewed gender ratio, Demographic Consequences
Housework: The invisible Labour
Women's Work: Its Politics and Economic Unrecognized and Unaccounted Work. Wages and Conditions of Work

UNIT III: ISSUES OF VIOLENCE AND GENDER STUDIES
Domestic Violence: Physical abuse, Mental abuse and Emotional disturbance
Consequences of domestic violence and legal Implications (Domestic Violence Act 2005- 498A)
Knowledge: Through the Lens of Gender
Unacknowledged Women and Men in Indian History- Women Scientist (Rupabai Furdoonji), Early Aviators (Babur Mirza and Pingle Madhusudhan Reddy), and Women Leader (T N Sadalakshmi)
Life Sketches: Mary Kom, Chanda Kochar, Mother Tesera, and Durga Bai Deshmukh

UNIT IV: ENGINEERING ETHICS

Importance of Value Education, Understanding Social Factors, Morals, Values ,Family Values-Harmony, Respect, Caring; Sharing; Integrity; Honesty; Courage; Cooperation; Commitment; Empathy; Self Confidence; Character; Accountability; Loyalty; Confidentiality; and Attitude

Ethics and Ethical Principles, Ethical Theories, and their uses

Professional Ethics, Engineering Ethics, Code of Ethics, Moral Autonomy of Engineers, Engineer's Responsibility for safety and Risk

UNIT V: GLOBAL PERSPECTIVE

Distinguish between Bribes and Gifts; Occupational Crimes; Globalization- Cross-Cultural Issues; Environmental Ethics; Internet and Computer Codes of Ethics

Case Study:

Ethics in Military and Weapons Development-Ethics in Research work

UNIT VI: PERSONALITY DEVELOPMENT

Spirituality, Personality and Our Identity, Understanding Self, Happiness, Positive Thinking, Understanding responsibility towards Society.

Introduction to Yoga in India; Origin and Development; Theoretical understanding of yoga; Stress Management : Modern and Yogic perspectives; Tackling ill-effects of Frustration, Anxiety and Conflict through modern and Yogic methods; Meditation Techniques; Suryanamaskar; Pranayama.

TEXT BOOKS:

1. Indian Culture Values And Professional Ethics(For Professional Students) by Prof.P.S.R.Murthy ; B.S.Publications.
2. Professional Ethics and Human Values by M. Jayakumar, Published by University Science Press,
3. Telugu Academy, Hyderabad, 2015, Towards A World of Equals, A Bilingual Text Book on Gender.

REFERENCE BOOKS:

1. The Yoga Sutras of Patanjali by Swami Satchitananda
2. The Secret Power of Yoga by Nischala Joy Devi
3. Light on Pranayama by B.K.S. Iyengar

I Year – II Sem. M.Tech.(DSCE)

NETWORK SECURITY AND CRYPTOGRAPHY

(OPEN ELECTIVE)

Code : 6ZC04

L	T	P	C
3	1	-	3

a	b	c	d	e	f
X	X				

After completing the course students are able to understand

CO1: Students will be familiar with Different types of security attacks, security mechanisms, security services, conventional Encryption model and techniques

CO2: After completion of this unit students will be aware of modern encryption techniques

CO3: Students will get about the topics which are technological centric fundamentals of conventional cryptography principles and algorithms

CO4: After completion of this unit students can understand to know how the message is provided authentication using hash functions

CO5: Students will be familiar with Significance of Digital signature and authentication protocols

CO6: After reading this unit students will aware of about the topics of Internet Protocol security

UNIT-I

Introduction:

Attacks, Services and Mechanisms, Security attacks, Security services, A Model for Internetwork security. Classical Techniques: Conventional Encryption model, Steganography, Classical Encryption Techniques.

UNIT-II

Modern Techniques:

Simplified DES, Block Cipher Principles, Data Encryption standard, Strength of DES, Differential and Linear Cryptanalysis, Block Cipher Design Principles and Modes of operations.

Algorithms: Triple DES, International Data Encryption algorithm, Blowfish, RC5, CAST-128, RC2, Characteristics of Advanced Symmetric block cifers.

UNIT-III

Conventional Encryption

Placement of Encryption function, Traffic confidentiality, Key distribution, Random Number Generation.

Public Key Cryptography

Principles, RSA Algorithm, Key Management, Diffie-Hellman Key exchange, Elliptic Curve Cryptography.

UNIT-IV

Number theory

Prime and Relatively prime numbers, Modular arithmetic, Fermat's and Euler's theorems, Testing for primality, Euclid's Algorithm, the Chinese remainder theorem, Discrete logarithms.

Message authentication and Hash functions:

Authentication requirements and functions, Message Authentication, Hash functions, Security of Hash functions and MACs.

UNIT-V

Hash and Mac Algorithms

MD File, Message digest Algorithm, Secure Hash Algorithm, RIPEMD-160, HMAC.

Digital signatures and Authentication protocols:

Digital signatures, Authentication Protocols, Digital signature standards.

Authentication Applications:

Kerberos, X.509 directory Authentication service. Electronic Mail Security: Pretty Good Privacy, S/MIME.

UNIT-VI

IP Security

Overview, Architecture, Authentication, Encapsulating Security Payload, Combining security Associations, Key Management.

Web Security

Web Security requirements, Secure sockets layer and Transport layer security, Secure Electronic Transaction.

Intruders, Viruses and Worms : Intruders, Viruses and Related threats.

Fire Walls : Fire wall Design Principles, Trusted systems.

TEXT BOOKS:

1. Cryptography and Network Security: Principles and Practice - William Stallings, 2000, PE.

REFERENCES:

1. Principles of Network and Systems Administration, Mark Burgess, John Wiel

I Year – II Sem. M.Tech.(DSCE)
SYSTEM-ON-CHIP ARCHITECTURE
(ELECTIVE III)

Code: 6T201

L	T	P	C
3	1	-	3

a	b	c	d	e	f
X	X	X			X

After completing the course students are able to understand

1.Understanding the abstraction in the hardware design. Learning the processor design and trade offs
2.Learning the architecture of ARM processor, execution of instructions
3.Learning how to programme a RAM processor with Architecture
4.Understanding the Memory concepts.
5.Understanding the structural support for the System Management.
6.Understanding the concepts of Operating systems.

Unit I: Introduction to processor design: Abstraction in hardware design, MUO a simple processor, Processor design trade off, design for low power consumption.

Unit II: ARM Processor as System-on-Chip: Acorn RISC machine – Architecture inheritance – ARM programming model – ARM development tools – 3 and 5 stage pipeline ARM organization – ARM instruction execution and implementation – ARM coprocessor interface.

Unit III: ARM assembly language programming: ARM instruction types – data transfer, data processing and control flow instructions – ARM instruction set – Coprocessor instructions.

Architectural support for high level language: Data types – abstraction in software design – Expressions – Loops – Functions and Procedures – Conditional statements – use of memory.

Unit IV: Memory Hierarchy: Memory size and speed – on chip memory – caches – cache design - an example – memory management.

Unit V: Architectural support for System Management: Advanced microcontroller bus architecture – ARM memory interface – ARM reference peripheral specification – Hardware system prototyping tools – Armulator – Debug architecture.

Unit VI: Architectural support for Operating System: An introduction to Operating Systems – ARM system control coprocessor – CP15 protection unit registers – ARM protection unit – CP15 MMU registers – ARM MMU architecture – Synchronization – Context switching input and output.

TEXT BOOKS

1. ARM System on Chip Architecture, Steve Furber, 2nd ed. 2000, Addison Wesley Professional.
2. Design of System on a Chip: Devices and Components, Ricardo Reis, 1st ed. 2004, Springer.

REFERENCE BOOKS

1. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology), Jason Andrews, Newnes, BK and CDROM.
2. System on Chip Verification: Methodologies and Techniques, Prakash Rasnikar, Peter Paterson and Leena Singh. L, 2001, Kluwer Academic Publisher.

I Year – II Sem. M.Tech.
CMOS ANALOG & MIXED SIGNAL DESIGN
(Elective-III)

Code: 6U203

L	T	P	C
3	1	-	3

a	b	c	d	e	f
X	X				

After completing the course students are able to understand

1. *Understanding basic circuit connections, functionality and their objectives.*
   Learning the procedures involved in Current Mirror, matching in MOSFET mirrors.Voltage dividers, band gap voltage references, referenced Self-biasing.
2. *Understanding the design and functioning of Amplifiers and Feedback Amplifiers and their stability.*
3. *Understanding the design and functioning of different types of Differential Amplifiers and their merits and demerits.*
4. *Understanding the design and functioning of Operational Amplifiers like basic CMOS Op-Amp, OTA.*
5. *Learning the Non-Linear & Dynamic Analog Circuits and their designing and Applications.*
6. *Learning the Data Converter Fundamentals, DAC & ADC specifications, Mixed Signal Layout issues, DAC architectures, ADC architectures*

A. CMOS ANALOG CIRCUITS:

Unit I
CURRENT SOURCES, SINKS & REFERENCES
The cascode connection, sensitivity and temperature analysis, transient response, layout of simple Current Mirror, matching in MOSFET mirrors, other Current Sources/Sinks.
Voltage dividers, current source self-biasing.

Unit II
AMPLIFIERS & FEEDBACK AMPLIFIERS
Gate Drain connected loads, Current Source Loads, Noise and Distortion, Class AB Amplifier.
Feedback Equation, properties of negative feedback and amplifier design, feedback topologies, amplifiers employing the four types of feedback, Stability.

Unit III
DIFFERENTIAL AMPLIFIERS
The Source Coupled pair, the Source Cross-Coupled pair, cascode loads, Wide-Swing Differential Amplifiers.

Unit IV
OPERATIONAL AMPLIFIERS
Basic CMOS Op-Amp Design, Operational Transconductance Amplifiers, Differential Output Op-Amp.

B. MIXED SIGNAL CIRCUITS:

Unit V
NON-LINEAR & DYNAMIC ANALOG CIRCUITS
Basic CMOS Comparator Design, Adaptive Biasing, Analog Multipliers, MOSFET Switch, Switched Capacitor circuits: Switched Capacitor Integrator, dynamic circuits.

Unit VI
DATA CONVERTER ARCHITECTURES
Data Converter Fundamentals, DAC & ADC specifications, Mixed Signal Layout issues, DAC architectures, ADC architectures.

TEXT BOOKS:

1. CMOS Circuit Design, Layout and Simulation - Baker, Li, Boyce, PHI, 2004.

REFERENCE BOOKS:

1. Analog Integrated Circuit Design - David A. Johns, Ken Martin, 1997, John Wiley & Sons
2. Design of Analog CMOS Circuits – B. Razavi, MGH, 2003, TMH.
3. Analog MOS ICs for Signal Processing – R.Gregorian, Gabor C. Temes, John Wiley & Sons

I Year – II Sem. M.Tech.(DSCE)
DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES
(ELECTIVE III)

Code: 6U204

L	T	P	C
3	1	-	3

a	b	c	d	e	f
X	X	X			

After completing the course students are able to understand

1. Analyse DSP tools such as DFT, FFT and systems such as LTI, LTV using MATLAB.
2. Obtain and understand the dynamic range, precision, conversional errors and computational errors
3. Learn basic architectural features and building blocks of Digital signal processor.
4. Understand and apply Execution control like hardware looping, interrupts and pipelining etc., analyze the processor TMS320C54XX processor.
5. Implement various DSP algorithms on TMS320C54XX.
6. Interface Memory and I/O peripherals to programmable DSP devices.

Unit I
INTRODUCTION TO DIGITAL SIGNAL PROCESING
Introduction, A Digital signal-processing system, The sampling process, Discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation, Analysis and Design tool for DSP Systems MATLAB, DSP using MATLAB.

Unit II
COMPUTATIONAL ACCURACY IN DSP IMPLEMENTATIONS
Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

Unit III
ARCHITECTURES FOR PROGRAMMABLE DSP DEVICES
Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External interfacing.

Unit IV
EXECUTION CONTROL AND PIPELINING
Hardware looping, Interrupts, Stacks, Relative Branch support, Pipelining and Performance, Pipeline Depth, Interlocking, Branching effects, Interrupt effects, Pipeline Programming models.
PROGRAMMABLE DIGITAL SIGNAL PROCESSORS
Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX processors, Pipeline Operation of TMS320C54XX Processors.

Unit V
IMPLEMENTATIONS OF BASIC DSP ALGORITHMS
The Q-notation, FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, PID Controller, Adaptive Filters, 2-D Signal Processing.
IMPLEMENTATION OF FFT ALGORITHMS
An FFT Algorithm for DFT Computation, A Butterfly Computation, Overflow and scaling, Bit-Reversed index generation, An 8-Point FFT implementation on the TMS320C54XX, Computation of the signal spectrum.
Unit VI
INTERFACING MEMORY AND I/O PERIPHERALS TO PROGRAMMABLE DSP DEVICES
Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).
A Multichannel buffered serial port (McBSP), McBSP Programming, a CODEC interface circuit, CODEC programming, A CODEC-DSP interface example.

TEXT BOOKS

1. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.
2. DSP Processor Fundamentals, Architectures & Features – Lapsley et al. S. Chand & Co, 2000.

REFERENCES

1. Digital Signal Processors, Architecture, Programming and Applications – B. Venkata Ramani and M. Bhaskar, TMH, 2002.
2. Digital Signal Processing – Jonatham Stein, John Wiley, 2005.

I Year – II Sem. M.Tech.(DSCE)
MEMS AND NEMS
(ELECTIVE III)

Code: 6UC02

L	T	P	C
3	1	-	3

a	b	c	d	e	f
x	x				

After going through the course, the student will be able to

1. *Understand concepts of micro-electro mechanical devices*
2. *Gain knowledge about . the fabrication process of microsystems*
3. *Understand. design concepts of micro sensors*
4. *Understand. design concepts of micro actuators*
5. *Understand . concepts of nano systems*
6. *Understand concepts of quantum mechanics*

UNIT I OVERVIEW AND INTRODUCTION
New trends in Engineering and Science: Micro and Nanoscale systems Introduction to Design of MEMS and NEMS, Overview of Nano and Microelectromechanical Systems, Applications of Micro and Nanoelectromechanical systems, Microelectromechanical systems, devices and structures Definitions, Materials for MEMS: Silicon, silicon compounds, polymers, metals

UNIT II MEMS FABRICATION TECHNOLOGIES
Microsystem fabrication processes: Photolithography, Ion Implantation, Diffusion, Oxidation. Thin film depositions: LPCVD, Sputtering, Evaporation, Electroplating; Etching techniques: Dry and wet etching, electrochemical etching; Micromachining: Bulk Micromachining, Surface Micromachining, High Aspect-Ratio (LIGA and LIGA-like) Technology; Packaging: Microsystems packaging, Essential packaging technologies, Selection of packaging materials

UNIT III MICRO SENSORS
MEMS Sensors: Design of Acoustic wave sensors, resonant sensor, Vibratory gyroscope, Capacitive and Piezo Resistive Pressure sensors- engineering mechanics behind these Micro sensors. Case study: Piezo-resistive pressure sensor

UNIT IV MICRO ACTUATORS
Design of Actuators: Actuation using thermal forces, Actuation using shape memory Alloys, Actuation using piezoelectric crystals, Actuation using Electrostatic forces (Parallel plate, Torsion bar, Comb drive actuators), Micromechanical Motors and pumps. Case study: Comb drive actuators

UNIT V CHEMICAL AND BIO MEDICAL MICRO SYSTEMS
Sensing mechanism & principle, membrane-transducer materials, chem.-lab-on-a-chip (CLOC) chemoresistors, chemocapacitors, chemotransistors, electronic nose (E-nose), mass sensitive chemosensors, fluroscence detection, calorimetric spectroscopy.

UNIT VI NANOSYSTEMS AND QUANTUM MECHANICS
Atomic Structures and Quantum Mechanics, Molecular and Nanostructure Dynamics: Shrodinger Equation and Wavefunction Theory, Density Functional Theory, Nanostructures and Molecular Dynamics, Electromagnetic Fields and their quantization, Molecular Wires and Molecular Circuits

REFERENCES:
1. Marc Madou, “Fundamentals of Microfabrication”, CRC press 1997.
2. Stephen D. Senturia,” Micro system Design”, Kluwer Academic Publishers,2001
Download link -
https://drive.google.com/file/d/0BzoKWH8M1BoTZ0Y4R2sxc0Vab28/view?usp=sharing
3. Tai Ran Hsu ,”MEMS and Microsystems Design and Manufacture” ,Tata Mcraw Hill, 2002.

Tai Ran Hsu Lectures Download Link -
https://drive.google.com/folderview?id=0BzoKWH8M1BoTRm5SZGJ4VDd6M0k&usp=sharing
Tai Ran Hsu Solution Manual Download link -
https://drive.google.com/file/d/0BzoKWH8M1BoTLVVGUmlnR0lmVTQ/view?usp=sharing
4. Chang Liu, "Foundations of MEMS", Pearson education India limited, 2006,
5. Sergey Edward Lyshevski, "MEMS and NEMS: Systems, Devices, and Structures" CRC Press, 2002.Download link -
https://drive.google.com/file/d/0BzoKWH8M1BoTN1c1eDRudmNzU1E/view?usp=sharing

I Year – II Sem. M.Tech.(DSCE)
Ad Hoc and Wireless Sensor Networks
(ELECTIVE III)

Code: 6U206

L	T	P	C
3	1	-	3

a	b	c	d	e	f
X	X	X			

By the end of this course, students will be able to

1. *Understand basics of Ad hoc Wireless Networks, MAC protocols for Ad hoc Wireless Networks.*
2. *Understand Routing protocols for Ad hoc Wireless Networks.*
3. *Understand Wireless sensor Networks.*
4. *Understand different routing techniques.*
5. *Understand the basics and issues of Wireless Sensor Networks.*
6. *Understand the difference and details of Random vs. structured Wireless Sensor Networks.*

Unit I
Ad Hoc Networks:
Characteristics and Applications of Ad hoc Networks, Routing – Need for routing and routing, classifications, Table Driven Routing Protocols, Source Initiated On-Demand

Unit II
Routing Protocols, Hybrid, Protocols – Zone Routing, Fisheye Routing, LANMAR for MANET with group mobility, Location Added Routing, Distance Routing Effects, Microdiscovery and Power Aware Routing.

Unit III
Wireless Sensor Networks:
Wireless Sensor Networks, DARPA Efforts, Classification, Fundamentals of MAC, Flat routing.

Unit IV
Routing:
Directed Diffusion, SPIN, COGUR, Hierarchical Routing, Cluster base routing,

Unit V
Scalable Coordination, LEACH, TEEN, APTEEN and Adapting to the dynamic nature of Wireless Sensor Networks.

Unit VI
Random vs structured WSN:
Localization, Hierarchy , organization, Stationary vs. mobile, Energy efficient routing, sleeping modes, issues in WSNs.

Books Recommended

1. D.P. Agrawal and Qing-An zeng, “Introduction to Wireless and Mobile Systems” Thomson Learning
2. Martyn Mallick, Mobile and Wireless Design Essentials, Wiley, 2003
3. Kavesh Pahlavan and Prashant Krishnamurty - “Principles of Wireless Networks – A Unified Approach, Pearson Education, 2002

I Year – II Sem. M.Tech (DSCE)
EMBEDDED SYSTEMS LAB

Code: 6U271

L	T	P	C
-	-	3	2

a	b	c	d	e	f
X	X	X		X	X

After going through the Laboratory course, the student will be able to

1. *Write the basic assembly language and Embedded C programs for timer, serial communication etc.*
2. *Interface various devices such as keyboard, ADC, DAC, LCD, Stepper Motor with 8051 microcontroller.*
3. *Study the Real Time Operating Systems and its applications.*
4. *Develop the device drivers for RT Linux.*
5. *Develop the Serial Communication drivers for ARM processor.*
6. *Design of RTOS kernel and study of Compile/Assembler.*

Research Methodology:
Research Methodology: An Introduction; Defining the Research Problem; Overview of – (i) Research Design, (ii) Sampling Design, (iii) Measurement and Scaling Techniques, (iv) Methods of Data Collection, (v) Processing and Analysis of Data, (vi) Interpretation and Report Writing.

Text Books:
1. Research Methodology: Methods and Techniques, C.R. Kothari, 2nd ed. New Age International.
2. Research in Education, Best & Kahn, 9th ed. 2006, PHI

LIST OF EXPERIMENTS:

CYCLE 1 : 8051 MICROCONTROLLERS

Serial data Transmission using 8051 microcontroller in different modes

Look up tables for 8051

Timing subroutines for 8051 – Real time and applications

Keyboard interface to 8051

ADC, DAC interface to 8051

LCD interface to 8051

CYCLE 2 :

Study of Real Time Operating Systems

Development of Device Drivers for RT Linux

Software Development for DSP Applications

Serial Communication Drivers for ARM Processors

Case Studies : Any Two –

Design of RTOS Kernel

Cross Compiler / Assembler

Vx Works

I Year -II Sem M.Tech. (DSCE)
LITERATURE REVIEW SEMINAR - 2

Code: 6U272

L	T	P	C
-	-	3	1

Max. Marks: 100

a	b	c	d	e	f
X	X		X	x	

After studying this course, the students will be able to

1. Identify a research topic
2. Collect literature
3. Write technical review paper
4. Present seminar
5. Discuss the queries and Publish research paper

Student shall collect the literature on a topic and critically review the literature and submit it to the Department in a report form, under the supervision of a faculty member and shall make an oral presentation before the Departmental Committee, which consists of the Head of the Department, a senior Faculty Member and the Supervisor, who will jointly evaluate the report and presentation. For each Seminar there will be only internal evaluation of 100 marks. A candidate has to secure a minimum of 50% to be declared successful.

In the First semester the report must be in the form of the review paper with a format used by IEEE / ASME etc. In the Second semester Technical Seminar in the form of Independent Review Paper must be of high quality fit for publication in a reputed conference / journal.

The evaluation format for seminar is as follows:

- Day to day evaluation by the Supervisor : 20 marks
- Final Report : 30 marks
- Presentation : 50 marks

A Student has to concentrate on the following sections while writing technical paper or presenting seminar.

Contents:

- Identification of specific topic
- Analysis
- Organization of modules
- Naming Conventions
- Writing style
- Figures
- Feedback
- Writing style
- Rejection
- Miscellaneous

REFERENCES:

1. Teach Technical Writing in Two Hours per Week by Norman Ramsey

2. For Technical Seminar the student must learn few tips from sample seminars and correcting himself, which is continues learning process

REFERENCE LINKS:

1. http://www.cs.dartmouth.edu/~scot/givingTalks/sld001.htm
2. http://www.cse.psu.edu/~yuanxie/advice.htm
3. http://www.eng.unt.edu/ian/guides/postscript/speaker.pdf

NOTE: A student can use any references for this process, but must be shared in classroom.

I Year – II Sem. M.Tech.(DSCE)
PROJECT SEMINAR - 1

Code: 6U273

L	T	P	C
-	-	-	2

Max. Marks: 100

a	b	c	d	e	f
X	X		X	x	x

The evaluation for the project seminar shall be done in two stages, i.e. in the middle of the semester and at the end of the semester. The evaluation process is as follows:

1 Topic : 20M

2 Presentation:30M

3 Report: 20M

4 Internal Evaluation:30M

A candidate shall secure a minimum of 50% to be declared successful.

I Year –II Sem. M.Tech.(DSCE)
COMPREHENSIVE VIVA-VOCE - 2

Code: 6U274

L	T	P	C
-	-	-	1

Max. Marks: 100

a	b	c	d	e	f
X			x		x

The Comprehensive Viva-Voce will be conducted by a Committee consisting of Head of the Department and two Senior Faculty members of the Department. The Comprehensive Viva-Voce is aimed to assess the students understanding in various subjects he/she studied during the M.Tech course of study. The Comprehensive Viva-Voce is valued for 100 marks by the Committee.

The internal marks for the Comprehensive Viva-Voce are 50 and external marks are 50 marks. A candidate has to secure a minimum of 50% to be declared successful.

II Year – I Sem. M.Tech.(DSCE)
PROJECT SEMINAR - 2

Code: 6U371

L	**T**	**P**	**C**
-	**-**	**-**	**2**

Max. Marks: 100

a	b	c	d	e	f
X	X		X	X	X

The evaluation for the project seminar shall be done in two stages, i.e. in the middle of the semester and at the end of the semester. The evaluation process is as follows

1 Topic : 20M

2 Presentation:30M

3 Report: 20M

4 Internal Evaluation:30M

A candidate shall secure a minimum of 50% to be declared successful.

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II Year – I Sem. M.Tech (DSCE)
Project work (Part 1)
Project status report

Code: 6U372

L	T	P	C
-	-	-	**20**

a	b	c	d	e	f
X	X	X	X	X	X

Every candidate is required to submit thesis or dissertation after taking up a topic approved by the Project Review Committee.

A Project Review Committee (PRC) shall be constituted comprising of Heads of all the Departments which are offering the M.Tech programs and three other senior faculty members concerned with the M.Tech. programme.

Registration of Project Work: A candidate is permitted to register for the project work after satisfying the attendance requirement of all the previous semesters and after obtaining the approval of the PRC.

A candidate has to submit, in consultation with his project supervisor, the title, objective and plan of action of his project work to the PRC for its approval. Only after obtaining the approval of PRC the student can initiate the Project work. This process is to be completed within four weeks of commencement of II year I semester.

The student shall submit a project report at the end of II year I semester, and the same shall be evaluated at the end of that semester by the PRC as Excellent/Good/Satisfactory/Unsatisfactory. In the case of Unsatisfactory declaration, the student shall re-submit the Project report after carrying out the necessary modifications / additions in the Project work, within the specified time as suggested by the PRC.

II Year – II Sem. M.Tech.(DSCE)
PROJECT SEMINAR - 3

Code: 6U471

L	T	P	C
-	-	-	2

Max. Marks: 100

a	b	c	d	e	f
X	X		X	X	X

The evaluation for the project seminar shall be done in two stages, i.e. in the middle of the semester and at the end of the semester. The evaluation process is as follows:

1 Topic : 20M
2 Presentation:30M
3 Report: 20M
4 Internal Evaluation:30M
A candidate shall secure a minimum of 50% to be declared successful.

II Year – II Sem. M.Tech.(DSCE)
PRE SUBMISSION SEMINAR

Code: 6U472

L	T	P	C
-	-	-	2

Max. Marks: 100

a	b	c	d	e	f
X	X		X		X

The evaluation for the project seminar shall be done in two stages, i.e. in the middle of the semester and at the end of the semester. The evaluation process is as follows:

1 Topic : 20M
2 Presentation:30M
3 Report: 20M
4 Internal Evaluation:30M
A candidate shall secure a minimum of 50% to be declared successful.

II Year – II Sem. M.Tech (DSCE)
PROJECT WORK AND DISSERTATION

Code: 6U473

L	T	P	C
-	-	-	**20**

a	b	c	d	e	f
X	X	X	X	X	X

By the end of this course, students will be able to

1.Critically and theoretically analyze the systems/products they are going to design or develop.
2.Apply the theoretical knowledge gained to bring out innovative products.
3.Effectively communicate in a variety of forms including written, visual, verbal, online and technical literacy.
4.Work and participate as effective members in a group within a professional environment.
5.Develop an ongoing critical awareness of learning needs in the application of appropriate technologies.
6.Gain as much knowledge and experience in areas of the area of Digital Systems and Computer Electronics

A candidate is permitted to submit Project Dissertation only after successful completion of PG subjects (theory and practical), seminars, Comprehensive viva-voce, PG Project Part–I, and after the approval of PRC, not earlier than 40 weeks from the date of registration of the project work. For the approval of PRC the candidate shall submit the draft copy of thesis to the Head of the Department and shall make an oral presentation before the PRC. Along with the draft thesis the candidate shall submit draft copy of a paper in standard format fit for publication in Journal / Conference, based on the project thesis, to the Head of the Department with due recommendation of the supervisor.

- Four copies of the Project Dissertation certified by the Supervisor and Head of the Department shall be submitted to the College.

- The dissertation shall be adjudicated by one examiner selected by the College. For this, Head of Department shall submit a panel of 3 examiners, who are eminent in that field, with the help of the PRC. The Chief Superintendent of the college in consultation with the college academic committee shall nominate the examiner.

- If the report of the examiner is not favorable, the candidate shall revise and resubmit the Dissertation, in the time frame as prescribed by PRC. If the report of the examiner is unfavorable again, the thesis shall be summarily rejected. The candidate can re-register only once for conduct of project and evaluation of Dissertation, and will go through the entire process as mentioned above. The total duration for the M.Tech program is limited to four years.

- If the report of the examiner is favorable, viva-voce examination shall be conducted by a Board consisting of the Head of the Department, Supervisor and the Examiner who adjudicated the Dissertation. The Board shall jointly report the student's performance in the project work as – (a) Excellent, or (b) Good, or (c) Satisfactory, or (d) Unsatisfactory, as the case may be. In case, the student fails in the viva-voce examination, or gets the Unsatisfactory grade, he can re-appear only once for the viva-voce examination, as per the recommendations of the Board. If he fails at the second viva-voce examination, the candidate can re-register only once for conduct of project and evaluation of Dissertation, and will go through the entire process as mentioned above. The total duration for the M.Tech program is limited to four years.