

**COURSE STRUCTURE
AND
DETAILED SYLLABUS
for
M.Tech course
in
DIGITAL SYSTEMS & COMPUTER ELECTRONICS
(ECE)**
(Applicable for the batches admitted from 2015-2016)



Department of Electronics and Communication Engineering

SREENIDHI INSTITUTE OF SCIENCE & TECHNOLOGY

(An Autonomous Institution approved by UGC and affiliated to JNTUH)

(Accredited by NAAC with 'A' Grade, Accredited by NBA of AICTE, Recipient of WBA under TEQIP I & II)

Yamnapet, Ghatkesar, R.R.District-501 301

M.Tech. (Digital Systems & Computer Electronics)
Course Structure and Syllabus
Academic Regulations: 2015-16

I YEAR - I Semester

Sl. No.	Code	Subject	L	T	P	Credits	Internal marks	External marks
1.	5U101	Digital System Design	3	1	-	3	25	75
2.	5U102	Advanced Data Communications	3	1	-	3	25	75
3.	5U103	Advanced Microprocessors and Microcontrollers	3	1	-	3	25	75
4.	5T101	VLSI Technology and Design	3	1	-	3	25	75
5.	5U104 5U105 5S110	Elective-I	3	1	-	3	25	75
6.	5T102 5S124	Elective-II	3	1	-	3	25	75
7.	5S125	Research Methodology	2	-	-	2	25	75
8.	5U171	Simulation Lab (VHDL)	-	-	4	2	25	75
9.	5U172	Literature Review Seminar -1	-	-	3	1	100	-
10.	5U174	Comprehensive Viva-Voce-1	-	-	-	1	100	-
		Total	20	6	7	24	400	600

I YEAR - II Semester

Sl. No.	Code	Subject	L	T	P	Credits	Internal marks	External Marks
1.	5S223	Advanced Computer Architecture	3	1	-	3	25	75
2.	5T106	Low Power VLSI Design	3	1	-	3	25	75
3.	5U201	Design of Fault Tolerant Systems	3	1	-	3	25	75
4.	5T202	Embedded Real Time Operating Systems	3	1	-	3	25	75
5.	5ZC47 5S120 5S221 5S222	Open Elective	3	1	-	3	25	75
6.	5T201 5U202 5U203 5U204	Elective-III	3	1	-	3	25	75
7.	5U271	Embedded Systems Lab	-	-	4	2	25	75
8.	5U272	Literature Review Seminar -2	-	-	3	1	100	-
9.	5U273	Project Seminar-1(Abstract)	-	-	3	2	100	-
10.	5U274	Comprehensive Viva-Voce-2	-	-	-	1	100	-
		Total	18	6	10	24	475	525

M.Tech. (Digital Systems & Computer Electronics)
Course Structure and Syllabus
Academic Regulations : 2015-16

II YEAR – I Semester

Sl. No.	Code	Subject	L	T	P	Credits	Internal Marks	External Marks
1.	5U371	Project Seminar-2 (Design and Development)	-	-	-	2	100	-
3.	5U372	Project Work (Part I) Project Status Report	-	-	-	20	Grading*	-
Total			-	-	-	22	100	-

*Grading – Excellent/ Good/ Satisfactory/ Unsatisfactory

II YEAR – II Semester

Sl. No.	Code	Subject	L	T	P	Credits	Internal Marks	External Marks
1.	5U471	Project Seminar-3 (Impementation/ Execution)	-	-	-	2	100	-
	5U472	Pre submission Seminar	-	-	-	2	100	-
2.	5U473	Project Work and Dissertation	-	-	-	20	-	Grading*
Total			-	-	-	24	200	-

*Grading – Excellent/ Good/ Satisfactory/ Unsatisfactory

ELECTIVE I

- 1) 5U104 - Advanced Digital Signal Processing
- 2) 5U105 - Image & Video Processing
- 3) 5S110 - Advanced Computer Networks
- 4) 5T103 - Hardware Software Co-Design
- 5) 5T112 - Embedded Networking
- 6) 5T108 - Hardware Description Languages and FPGA Based Design

ELECTIVE II

- 1) 5T102 - CPLD & FPGA Architectures and Applications
- 2) 5S124 - Internetworking
- 3) 122EP21 - Digital Control Systems
- 4) 5T110 - Embedded Control Systems
- 5) 5U106 - Embedded Systems for Wireless and Mobile Communications
- 6) 5T111 - CAD for VLSI Circuits
- 7) 5T204 - Testing of VLSI Circuits

OPEN ELECTIVE

- 1) 5ZC13 - Entrepreneurship and Innovation
- 2) 5ZC03 - Banking Operation, Insurance and Risk Management
- 3) 5H233 - Ethics, Morals, Gender sensitization and Yoga
- 4) 5QC33 - Intellectual and Property Rights

ELECTIVE III

- 1) 5T201 - System on Chip Architecture
- 2) 5U202 - CMOS Analog & Mixed Signal Design
- 3) 5U203 - Digital Signal Processors and Architectures
- 4) 5U204 - Radar Signal Processing
- 5) 5U205 - Adhoc & Wireless Sensor Networks
- 6) 5U206 - RF System Design

**I Year -I Sem M.Tech. (DSCE)
DIGITAL SYSTEM DESIGN**

Code : 5U101

L T P C
3 1 - 3

a	b	c	d	e	f	g	h	i	j	k
x	X		X							X

After studying this course, the students will be able to

1. Understand designing with Programmable Devices such as PLA, PAL, ROM and FPGAs.
2. Understand the representation and implementation of sequential circuit with State Machine Charts, explained with examples.
3. Understand the significance of Design For Testability due to faults with introduction to fault modelling and different techniques to detect single stuck at fault.
4. Understand different test pattern generation techniques to detect faults.
5. Understand Techniques on fault diagnosis, minimization and transformation of sequential circuits
6. Understand Minimizing design implementation space of a PLA by using folding technique and fault modeling in a PLA

Unit-I: Designing with Programmable Logic Devices

Designing with Read only memories – Programmable Logic Arrays – Programmable Array logic – Sequential Programmable Logic Devices – Design with FPGA's– Using a One-hot state assignment,

State transition table- State assignment for FPGA's - Problem of Initial state assignment for One –Hot encoding - State Machine charts – Derivation of SM Charts – Realization of SM charts – Design Examples –Serial adder with Accumulator - Binary Multiplier – Dice Game controller – Binary Divider – Control logic for Sequence detector – Realization with Multiplexer – PLA – PAL.

Unit-II: Fault Modeling

Logic Fault model – Fault detection & Redundancy- Fault equivalence and fault location – Fault dominance – Single stuck at fault model – Multiple stuck at fault models –Bridging fault model

Fault diagnosis of combinational circuits by conventional methods – Path sensitization techniques, Boolean Difference method – Kohavi algorithm, Test Algorithms- D-Algorithm.

Unit-III: Test Pattern Generation

Random testing, Transition count testing, Exhaustive Testing and Pseudo Random Testing. Signature analysis and test bridging faults.

Unit-IV: Fault Diagnosis in Sequential Circuits

Circuit Test Approach, Transition Check Approach - State identification and fault detection experiment, Machine identification, Design of fault detection experiment.

Unit-V: PLA Minimization and Testing

PLA Minimization – PLA folding, Fault model in PLA, Test generation and Testable PLA Design.

Unit-VI: Minimization and Transformation of Sequential Machines

The Finite state Model – Capabilities and limitations of FSM – State equivalence and machine minimization – Simplification of incompletely specified machines.

Fundamental mode model – Flow table – State reduction – Minimal closed covers – Races, Cycles and Hazards.

TEXT BOOKS:

1. Fundamentals of Logic Design – Charles H. Roth, 5th ed., Cengage Learning.
2. Digital Systems Testing and Testable Design – Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman- John Wiley & Sons Inc.
3. Switching and Finite Automata Theory – Z. Kohavi , 2nd ed., 2001, TMH
4. Logic Design Theory – N. N. Biswas, PHI

REFERENCES :

1. Digital Design – Morris Mano, M.D.Ciletti, 5^{T^h} Edition, PHI.
2. Digital Circuits and Logic Design –Samuel C. Lee, PHI

**I Year -I Sem M.Tech.(DSCE)
ADVANCED DATA COMMUNICATIONS**

Code: 5U102

L T P C
3 1 - 3

a	b	c	d	e	f	g	h	i	j	k
X	X	X	X					X		

After studying this course, the students will be able to

1. Describe and determine the performance of different digital modulation techniques for digital data transmission over the channel.
2. Describe data communication system model and different networks for transmission of digital data with different transmission modes and rates.
3. Describes the different error detection and correction schemes for transmission of digital information over the channel.
4. Describes the functions of Data Link control and design formats of various Data Link Protocols.
5. Describes different switching and multiplexing techniques for transmission of digital data.
6. Describe and determine the performance of Random access, controlled access and channelization protocols.

Unit-I:

Digital Modulation: Introduction, Information Capacity Bits, Bit Rate, Baud, and M-ARY Coding, ASK, FSK, PSK, QAM, BPSK, QPSK, 8PSK, 16PSK, 8QAM, 16QAM, DPSK – Methods, Band Width Efficiency, Carrier Recovery, Clock Recovery.

Applications: Ethernet

Unit -II:

Basic Concepts of Data Communications, Interfaces and Modems: Data Communication-Components, Networks, Distributed Processing, Network Criteria- Applications, Protocols and Standards, Standards Organizations- Regulatory Agencies, Line Configuration- Point-to-point- Multipoint, Topology- Mesh- Star- Tree- Bus- Ring- Hybrid Topologies, Transmission Modes- Simplex- Half duplex- Full Duplex, Categories of Networks- LAN, MAN, WAN and Internetworking, Digital Data Transmission- Parallel and Serial, DTE- DCE Interface- Data Terminal Equipment, Data Circuit- Terminating Equipment, Standards EIA 232 Interface, Other Interface Standards, Modems- Transmission Rates.

Unit-III:

Error Detection and Correction: Types of Errors- Single- Bit Error, CRC (Cyclic Redundancy Check)- Performance, Checksum, Error Correction- Single-Bit Error Correction, Hamming Code.

Unit-IV:

Data link Control: Stop and Wait, Sliding Window Protocols.

Data Link Protocols: Asynchronous Protocols, Synchronous Protocols, Character Oriented Protocol- Binary Synchronous Communication (BSC) - BSC Frames- Data Transparency, Bit Oriented Protocols – HDLC, Link Access Protocols.

Unit-V:

Switching: Circuit Switching- Space Division Switches- Time Division Switches- TDM Bus-Space and Time Division Switching Combinations- Public Switched Telephone Network, Packet Switching- Datagram Approach- Virtual Circuit Approach- Circuit Switched Connection Versus Virtual Circuit Connection, Message Switching.

Multiplexing: Time Division Multiplexing (TDM), Synchronous Time Division Multiplexing, Digital Hierarchy, Statistical Time Division Multiplexing.

Unit-VI:

Multiple Access: Random Access, Aloha- Carrier Sense Multiple Access (CSMA)- Carrier Sense Multiple Access with Collision Detection (CSMA)- Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA), Controlled Access- Reservation- Polling- Token Passing, Channelization- Frequency- Division Multiple Access (FDMA), Time - Division Multiple Access (TDMA), - Code - Division Multiple Access (CDMA).

Applications: GSM and WCDMA.

TEXT BOOKS:

1. Data Communication and Computer Networking - B. A.Forouzan, 3rd ed., 2008, TMH.
2. Advanced Electronic Communication Systems - W. Tomasi, 5 ed., 2008, PEI.

REFERENCES:

1. Data Communications and Computer Networks - Prakash C. Gupta, 2006, PHI.
2. Data and Computer Communications - William Stallings, 8th ed., 2007, PHI.
3. Data Communication and Tele Processing Systems - T. Housely, 2nd Edition, 2008, BSP.
4. Data Communications and Computer Networks- Brijendra Singh, 2nd ed., 2005, PHI.
5. Telecommunication System Engineering – Roger L. Freeman, 4/ed., Wiley-Interscience, John Wiley & Sons, 2004.

I Year – I Sem. M.Tech.(DSCE)
ADVANCED MICROPROCESSORS AND MICROCONTROLLERS

Code: 5U103

L T P C
3 1 - 3

a	b	c	d	e	f	g	h	i	j	k
X	X	X		X	X			X		X

After studying this course, the students will be able to

1. *Understand the architecture, interfacing , instruction set and programming of 8086 microprocessor.*
2. *Understanding of high end Processors of X86 family,Multi-tasking and Multi-user Operating System.*
3. *Understanding the interfacing, interrupts, DMA, and working of cache memory, co-processors.*
4. *Understanding basic architecture and development tools of ARM Processor.*
5. *Understanding of assembly language programmed and High Level Language support provided by ARM Processor.*
6. *Understanding the applications of microprocessor, microcontrollers, and ARM Processor and features of some standard serial interfaces.*

Unit-I

8086 microprocessor family overview, 8086 Internal Architecture, memory interfacing constructing the machine codes for 8086, Introduction to programming the 8086, writing programmes with Assembler, Assembly Language program development tools.

Unit-II

The 80286, 80386, 80486 and Pentium processors – The Intel 80286 microprocessor, The Intel 80386 32-Bit microprocessor architecture, The Intel 80486 microprocessor and pentium processor architecture concept of multiuser / multitasking operating system.

Unit-III

Interfacing to 8086 microprocessor, 8086 Interrupts and Interrupt applications, Digital Interfacing, Analog interfacing and Industrial Control, DMA, Cache Memory and co-processors.

Unit-IV

Introduction to ARM processor -Programming model – ARM Development Tools – ARM instruction set execution and implementation – ARM coprocessor interface. ARM Processor as System-on-Chip: Acorn RISC machine – Architecture inheritance –3 and 5 stage pipeline ARM organization.

Unit-V

ARM assembly language programming: ARM instruction types – data transfer, data processing and control flow instructions – ARM instruction set – Coprocessor instructions.

Architectural support for high level language: Data types – abstraction in software design – Expressions – Loops – Functions and Procedures – Conditional statements – use of memory.

Unit-VI

Simple applications of microprocessors and microcontrollers using ARM 9 processors, Robot control, stepper motor control, interfacing of analog and digital sensors, process control, measuring of parameters like – pressure, temperature, level, position, etc., using microcontrollers. Standard interfaces like Centronics, IEEE-488, USB and RS-232.

TEXT BOOKS:

1. Microprocessors and Interfacing by DOUGLAS V HALL, Revised Second Edition.
2. Computers and Components, Wayne Wolf, Elseveir.

REFERENCES:

1. ARM Technical references
2. Embedded System Design, Frank Vahid, Tony Givargis, John Wiley.
3. Microcontrollers, Raj Kamal, Pearson Education.
4. An Embedded Software Primer, David E. Simon, Pearson Education.

**I Year – I Sem. M.Tech. (DSCE)
VLSI TECHNOLOGY & DESIGN**

Code: 5T101

L	T	P	C
3	1	-	3

a	b	c	d	e	f	g	h	i	j	k
X	X	X		X						

After studying this course, the students will be able to

1. *Understand the fabrication processes and electrical properties of various MOSFET's, their advantages and disadvantages.*
2. *Able to draw the Layout diagrams and Stick diagrams for CMOS gates and Circuits etc. Also understand about the design rules required during drawing of Layout diagrams and Stick diagrams.*
3. *Understand about various alternative gate circuits and able to analyze delay and power dissipation in them.*
4. *Understand and analyse various delays and power consumption in the combinational circuits. Student also able to test various combinational gates and circuits for faults.*
5. *Understand the need of clocking disciplines required for proper operation of sequential systems and also able to analyse various delays and power consumption in the sequential circuits.*
6. *Understand the floor planning methods, power, clock distribution and off-chip connections of a chip.*

Unit – I:

REVIEW OF MICROELECTRONICS AND INTRODUCTION TO MOS TECHNOLOGY: MOS, CMOS, BiCMOS Technologies.

BASIC ELECTRICAL PROPERTIES OF MOS AND BICMOS CIRCUITS: I_{ds} versus V_{ds} relationships, MOS Transistor Threshold Voltage V_t , MOS Transistor Transconductance(g_m) and Output Conductance(g_{ds}), Pass Transistor, nMOS Inverter, Determination of pull-up to pull down ratio(Z_{pu}/Z_{pd}) for an nMOS inverter driven by another nMOS inverter, Determination of pull-up to pull down ratio(Z_{pu}/Z_{pd}) for an nMOS inverter driven through one or more pass transistors, Alternative forms of Pull-Up, The CMOS Inverter Latch-up in CMOS circuits, Bi CMOS Inverter.

Unit – II:

MOS TRANSISTOR PARASITICS: MOS Transistor circuit model.

LAYOUT DESIGN AND RULES: MOS Layers, Stick diagrams, Layout diagrams, Design rules for wires (nMOS and CMOS), ' λ ' based design rules, Transistor Design rules(nMOS, pMOS and CMOS), Vias, cut, Design rules for Contacts in NMOS ckts, Buried and butting contacts.

Unit – III:

LOGIC GATES: Static Complementary Gates-Gate structures, Logic levels, Delay and Transition time, Power consumption, The Speed-Power product, Driving large loads; Alternative Gate circuits-Pseudo nMOS logic, DCVS logic, Domino logic; Low power gates;

INTERCONNECTS: Estimation of Resistance, Capacitance and Inductance parasitic, Delay through Resistive interconnects-Lumped model, Lumped RC Tree model, Lumped RC ladder model, Distributed RC ladder model; Delay through Inductive interconnect-Transmission line model, Cross-talk between RC wires.

Unit – IV:

COMBINATIONAL LOGIC NETWORKS: Standard Cell Based Layout Design, Layout of Full Adder, Left edge algorithm, Combinational Network delay-Fanout delay, Path delay, delay due to false path, Transistor sizing, Cross-talk minimization, Power optimization, Combinational logic Testing-Gate Testing, Network testing.

Unit – V:

SEQUENTIAL SYSTEMS: Latches and Flip-Flops-Latch, Flip-Flop, Setup and Hold times, Dynamic Latch circuit, Multiplexed Dynamic Latch circuit, Recalculating Static latch circuit, Clocked inverter, A D-Latch built from clocked inverters, SR Flip-Flop, D-Flip-Flop; Sequential systems and Clocking disciplines-Clocking rule1, rule2, One phase systems for FFs, Two phase systems for Latches, Advanced clocking Analysis; Sequential system Design-Designing of one bit counter, Designing of a 01 string recognizer; State assignment-Encoding a Shift register, How state codes affect delay; Power optimization, Design validation and testing-LSSD.

Unit – VI:

HIGH DENSITY MEMORY ELEMENTS: Architecture of a high density memory system, ROM, Static RAM, Dual ported SRAM, One transistor Dynamic RAM, Three transistor dynamic RAM.

FLOOR PLANNING: Floor planning methods-Block placement and Channel definition, Wind mill structures, Global routing, switch box routing, Power distribution, Clock distribution;

OFF-CHIP CONNECTIONS: Packages, Power line inductance, I/O Architecture, Pad Design.

TEXT BOOKS:

1. Essentials of VLSI Circuits and Systems, K. Eshraghian, Douglas A.Pucknell, 2005, PHI.
2. Modern VLSI Design - Wayne Wolf, 3rd ed., 1997, Pearson Education.
3. Digital Integrated Circuits A Design Perspective – Jan M.Rabaey, Ananta Chandrakasan, Borivoje Nikolic, Pearson Education

REFERENCES:

1. Principles of CMOS VLSI Design A System Perspective – Neil H.E.Weste, K. Eshraghian, Addison-Wesley Publishing Company.
2. Introduction to VLSI Circuits and Systems – John Uyemura, John Willey & Sons, Inc
3. VLSI design techniques for Analog and Digital Circuits – Randall L.Geiger, Phillip E.Allen, Noel R.StraderMcGraw-Hill Company
4. Application Specific Integrated circuits – Sabastian Smith

I Year – I Sem. M.Tech.(DSCE)
ADVANCED DIGITAL SIGNAL PROCESSING
(ELECTIVE-I)

Code : 5U104

L T P C
3 1 - 3

a	b	c	d	e	f	g	h	i	j	k
X	X	X	X	X						

After going through the course, the student will be able to

1. Compute DFT and perform Linear Filtering ,Frequency Analysis of Signals using DFT.
2. Compute the Fast Fourier using the radix, Goertzel and Chrip-z Transform Algorithms.
3. Design IIR Filters using Butterworth and Chebyshev Approximations, and realise Structures for IIR Systems.
4. Design FIR Filters by several methods and realise Structures for FIR Systems
5. Define, represent, classify, analyse and also represent Multirate signal processing and its applications
6. Understand and predict both forward and backward linear predictors for optimum power estimation.

Unit I

DISCRETE FOURIER TRANSFORMS: Frequency domain Sampling, Properties of DFT, Linear Filtering Methods based on the DFT,Frequency Analysis of Signals using DFT.

Unit II

FAST FOURIER TRANSFORMS: Radix-2, Radix-4, Split Radix FFT Algorithms, The Goertzel Algorithm and Chrip-z Transform Algorithm.

Unit III

DESIGN OF IIR FILTERS: Design of IIR Filters using Butterworth and Chebyshev Approximations, Structures for IIR Systems –Direct Form, Cascade, Parallel, Lattice and Lattice-Ladder Structures.

Unit –IV

DESIGN OF FIR FILTERS: Fourier series method, Windowing Techniques, Design of Digital Filters based on Least-Squares Method, Structures for FIR Systems –Direct Form, Cascade, Lattice Structures.

Unit V

MULTIRATE SIGNAL PROCESSING: Introduction, Decimation by a factor D, Interpolation by a factor I, Sampling rate conversion by a rational factor I/D, Filter design & Implementation for sampling rate conversion.

Unit VI

Linear Prediction : Forward and Backward Linear Prediction – Forward Linear Prediction, Backward Linear Prediction, Optimum reflection coefficients for the Lattice Forward and Backward Predictors. Solution of the Normal Equations: Levinson Durbin Algorithm, Schur Algorithm. Properties of Linear Prediction Filters

TEXT BOOKS

Digital Signal Processing: Principles, Algorithms and Applications - J.G.Proakis & D.G.Manolokis, 5th ed., PHI.

1. Discrete Time signal processing - Alan V Oppenheim & Ronald W Schaffer, PHI.
2. DSP – A Practical Approach – Emmanuel C.Ifearcher, Barrie. W. Jervis, 2nd ed., Pearson Education.

REFERENCE BOOKS

1. Digital Spectral Analysis with applications– S. Lawrence Marple Jr, Prentice-Hall Series in Signal Processing.
2. Modern spectral Estimation : Theory & Application – S. M .Kay, 1988, PHI.
3. Multirate Systems and Filter Banks – P.P.Vaidyanathan – Pearson Education
4. Digital Signal Processing – S.Salivahanan, A.Vallavaraj, C.Gnanapriya, 2000,TMH

**I Year -I Sem M.Tech.(DSCE)
IMAGE & VIDEO PROCESSING
(ELECTIVE – I)**

Code : 5U105

L T P C
3 1 - 3

a	b	c	d	e	f	g	h	i	j	k
X	X	X	X	X						X

After studying this course, the students will be able to

1. *Get the knowledge of the basic step in image processing system, Discrete cosine transforms and discrete wave let transforms.*
2. *Differentiate image enhancement methods ,different types of spatial domain and frequency domain methods.*
3. *Get the knowledge of point, line and edge detection, thresholding , Region based segmentation.*
4. *Differentiate different types of redundancies, lossy and lossy less image compression, different types of coding techniques.*
5. *Know the difference between analog video and digital video, different types of image formation and sampling of video signals*
6. *Study the different types of motion estimation techniques and application of motion estimation in video coding.*

Unit I: Fundamentals of Image Processing and Image Transforms

Basic steps of Image Processing System Sampling and Quantization of an image – Basic relationship between pixels

Image Transforms: 2 D- Discrete Fourier Transform, Discrete Cosine Transform (DCT), Wavelet Transforms: Continuous Wavelet Transform, Discrete Wavelet Transforms.

Unit II: Image Enhancement

Spatial domain methods: Histogram processing, Fundamentals of Spatial filtering, Smoothing spatial filters, Sharpening spatial filters.

Frequency domain methods: Basics of filtering in frequency domain, image smoothing, image sharpening, Selective filtering.

Unit III: Image Segmentation & Compression

Image Segmentation concepts, Point, Line and Edge Detection, Thresholding and Region Based segmentation. Image compression fundamentals - Coding Redundancy, Spatial and Temporal redundancy, Compression models: Lossy & Lossless, Huffman coding, Arithmetic coding, LZW coding, Run length coding, Bit plane coding, Transform coding, Predictive coding.

Unit IV: Basic steps of Video Processing

Analog Video, Digital Video. Time-Varying Image Formation models: Three-Dimensional Motion Models, Geometric Image Formation, Photometric Image Formation, Sampling of Video signals and filtering operations.

Unit V: 2-D Motion Estimation

Optical flow, General Methodologies, Pixel Based Motion Estimation, Block- Matching Algorithm, Mesh based Motion Estimation, Global Motion Estimation, Application of motion estimation in Video coding.

Unit VI: Three dimensional Motion Estimation & Waveform based coding

Feature based motion estimation, Direct Motion Estimation. **Block based transform coding:** over view, one dimensional unitary transform, two dimensional unitary transform, The discrete cosine transform, Bit allocation and transform coding gain , **Predictive Coding:** over view, optimal predictor design and predictive coding gain, Block based hybrid video coding.

TEXT BOOKS

1. Digital Image Processing – Gonzaleze and Woods, 3rd ed., Pearson.
2. Video processing and communication – Yao Wang, Joem Ostermann and Ya–quin Zhang. 1st Ed., PH Int.

REFERENCE BOOKS

1. Digital Video Processing – M. Tekalp, Prentice Hall International

I Year – I Sem. M.Tech.(DSCE)
ADVANCED COMPUTER NETWORKS
(ELECTIVE – I)

Code: 5S110

								L	T	P	C
								3	1	-	3
a	b	c	d	e	f	g	h	i	j	k	

After completing the course students are able to

1. *Get the knowledge of congestion control Quality of Service and queue management.*
2. *Describes Wireless LAN topologies, and its requirements, the design issues and functions of physical layer, Medium access control (MAC) layer.*
3. *Describes Wireless Personal Area Networks , first generation to third generation Cellular systems, protocols and architecture of IEEE 802.16 standard and Wireless ATM.*
4. *Describes Cellular Systems and Infrastructure, Virtual Private network*
5. *Describes ATM Protocol Reference model ,ATM Traffic and Service Parameterization.*
6. *Describes Interconnection Networks and SONET architecture*

Unit – I

Congestion and Quality of Service (QoS): Data traffic congestion, congestion control, open loop and closed loop congestion control in TCP and Frame Relay, Quality of Service, Flow characterization, Flow classes, Need for QoS, Resource allocation, Best effort service features, Techniques to improve QoS.

Queue Management: Passive, active (RED), and Fair (BRED, choke) Queue management schemes, scheduling, traffic shaping, Resource reservation and Admission Control Scheduling, Integrated and Differential services.

Unit – II

Wireless Local Area Network: Introduction, Wireless LAN topologies, Wireless LAN requirements, the Physical layer, Medium access control (MAC) layer, Latest Developments.

Unit – III

Wireless Personal Area Networks (WPANs): Introduction to PAN technology and applications, Commercial alternatives – Bluetooth, Home RF.

Wireless Wide Area Networks and MANs: The cellular concept, Cellular architecture, First Generation Cellular systems, Second Generation Cellular systems, Third Generation Cellular systems, Wireless in Local Loop, Wireless ATM, IEEE 802.16 standard.

Unit – IV

Cellular Systems and Infrastructure – Based Wireless Networks: Cellular Systems Fundamentals, Channel Reuse, SIR and User Capacity, Interference reduction techniques, Dynamic resource allocation, Fundamental rate limits.

Virtual Private network (VPN): Types of VPN, VPN General Architecture, Current VPN advantages and disadvantages, VPN security issues, VPN standards.

Unit – V

ATM Protocol Reference Model: Introduction, Transmission Convergence (TC) sub-layer, Physical Medium Dependent (PMD) sub-layer, Physical layer standards for ATM.

ATM Layer: ATM Cell structure Header at UNI, ATM Cell structure Header at NNI, ATM Layer functions.

ATM Adaptation Layer: Service classes and ATM Adaptation layer, ATM Adaptation Layer 1 (AAL1), ATM Adaptation Layer 2 (AAL2), ATM Adaptation Layer 3/4 (AAL3/4), ATM Adaptation Layer 5 (AAL5).

ATM Traffic and Service Parameterization: ATM traffic parameters, ATM service parameters, Factors affecting QoS parameters, ATM service categories, QoS and QoS Classes.

Unit – VI: Interconnection Networks: Introduction, Banyan Networks – Properties, Crossbar switch, Three stage class networks, Rearrangeable networks, Folding algorithm, Benes networks, Looping algorithm, Bit-Allocation Algorithm.

SONET/SDH: SONET/SDH Architecture, SONET Layers, SONET Frames, STS Multiplexing, SONET Networks.

TEXT BOOKS:

1. Wireless Communications – Andrea Goldsmith, 2005, Cambridge University Press.
2. Ad Hoc Wireless Networks: Architectures and Protocols – C. Siva Ram Murthy and B.S. Manoj, 2004, PHI.
3. Data Communication and Networking - B.A. Forouzan, 2004, TMH.

REFERENCES:

1. Introduction to Broadband Communication Systems– Sadiku, Mathew N.O., Akujuobi, Cajetan M., PHI
2. Wireless Networks – P. Nicopolitidis, A.S. Pomportsis, G.I. Papadimitriou, M.S. Obaidat, 2003, John Wiley & Sons.
3. High Performance TCP / IP Networking – Mahaboob Hassan, Jain Raj, PHI.

**I Year – I Sem. M.Tech.(DSCE)
HARDWARE- SOFTWARE CO-DESIGN
(ELECTIVE-I)**

Code: 5T103

L T P C
3 1 - 3

a	b	c	d	e	f	g	h	i	j	k
X	X	X	X	X						

After going through the course, the student will be able to

- 1: Able to understand models, architecture, methodology and languages for co-design. Hardware-Software algorithms are studied
- 2: To understand Prototyping and emulation techniques, environments, future developments, architecture Specialization techniques and system communication infrastructure
- 3: Study of target architectures
- 4: Study of compilation technologies and tools for embedded processor architectures
- 5: Able to understand computational model, interfacing components, design and implementation verification, verification tools
- 6: Study of design representation for system level synthesis, system level specification languages

Unit –I**CO- DESIGN ISSUES**

Co- Design Models, Architectures, Languages, a Generic Co-design Methodology.

CO- SYNTHESIS ALGORITHMS

Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

Unit –II**PROTOTYPING AND EMULATION**

Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

Unit -III**TARGET ARCHITECTURES**

Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

Unit – IV**COMPILATION TECHNIQUES AND TOOLS FOR EMBEDDED PROCESSOR ARCHITECTURES**

Modern embedded architectures, embedded software development needs, compilation technologies practical consideration in a compiler development environment.

Unit – V

DESIGN SPECIFICATION AND VERIFICATION

Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

Unit – VI

LANGUAGES FOR SYSTEM – LEVEL SPECIFICATION AND DESIGN-I

System – level specification, design representation for system level synthesis, system level specification languages

LANGUAGES FOR SYSTEM – LEVEL SPECIFICATION AND DESIGN-II

Heterogeneous specifications and multi language co-simulation the cosyma system and lycos system.

TEXT BOOKS

1. Hardware / software co- design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – 2009, Springer.
2. Hardware / software co- design Principles and Practice, 2002, Kluwer Academic Publishers

I Year – I Sem. M.Tech.(DSCE)
EMBEDDED NETWORKING
(ELECTIVE – I)

Code: 5T112

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3 **1** **-** **3**

a	b	c	d	e	f	g	h	i	j	k
X	X	X	X		X			X		

After studying this course, the students will be able to

1. Understanding the signal conversion and processing, coding and quantization. Review of transforms
2. Applying transfer functions to digital systems and understanding the closed loop systems, multi rate systems and cyclic rate systems.
3. Understanding the controllability of LTI systems, and also learning how to increase the stability of a system.
4. Learning Time Domain and Z-Domain analysis and applying to the second order systems. Understanding different frequency domain analyses techniques.
5. Designing the discrete data control systems, data controllers and bilinear transformations.
6. Learning the state transition equations, computing the transition matrix and decomposition of discrete systems.

Unit I

EMBEDDED COMMUNICATION PROTOCOLS 9

Embedded Networking: Introduction – Serial/Parallel Communication – Serial communication protocols -RS232 standard – RS485 – Synchronous Serial Protocols –Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel port programming - ISA/PCI Bus protocols – Firewire.

Unit II

USB AND CAN BUS 9

USB bus – Introduction – Speed Identification on the bus – USB States – USB bus communication: Packets –Data flow types –Enumeration –Descriptors –PIC 18 Microcontroller USB Interface – C Programs –CAN Bus – Introduction - Frames –Bit stuffing –Types of errors –Nominal Bit Timing – PIC microcontroller CAN Interface –A simple application with CAN

Unit III

ETHERNET BASICS 9

Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components –Ethernet Controllers – Using the internet in local and internet communications – Inside the Internet protocol

Unit IV

EMBEDDED ETHERNET 9

Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP – Keeping Devices and Network secure.

Unit V

WIRELESS EMBEDDED NETWORKING 9

Wireless sensor networks – Introduction – Applications – Network Topology – Localization

Unit- VI

Time Synchronization - Energy efficient MAC protocols –SMAC – Energy efficient and robust routing – Data Centric routing.

REFERENCE BOOKS

1. Frank Vahid, Tony Givargis „Embedded Systems Design: A Unified Hardware/Software Introduction", John & Wiley Publications,2002
2. Jan Axelson, „Parallel Port Complete:Programming,interfacing and using the PC"s parallel printer port ,, , Penram publications, 1996.
3. Dogan Ibrahim, „Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series", Elsevier 2008.
4. Jan Axelson „Embedded Ethernet and Internet Complete", Penram publications, 2003.
5. Bhaskar Krishnamachari, „Networking Wireless Sensors", Cambridge press 2005.

I Year – I Sem. M.Tech.(DSCE)
Hardware Description Languages and FPGA Based Design
(ELECTIVE-I)

Code : 5T108

L T P C
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After going through the course, the student will be able to

1. Understanding the signal conversion and processing, coding and quantization. Review of transforms
2. Applying transfer functions to digital systems and understanding the closed loop systems, multi rate systems and cyclic rate systems.
3. Understanding the controllability of LTI systems, and also learning how to increase the stability of a system.
4. Learning Time Domain and Z-Domain analysis and applying to the second order systems. Understanding different frequency domain analyses techniques.
5. Designing the discrete data control systems, data controllers and bilinear transformations.
6. Learning the state transition equations, computing the transition matrix and decomposition of discrete systems.

Unit-I

Verilog : basic concepts- Lexical conventions, data types, system tasks and compiler directives. Modules and ports. Gate level modeling- gate types, various types of gate delay specifications.

Unit-II

Data flow modeling- assignments, delays, expressions, operators, Behavioral modeling- structured procedures, procedural assignments, timing controls, conditional statements, loops, sequential and parallel blocks, generate blocks. Tasks and functions

Unit-III

FPGA Architectures and Technology. Historical background, channel type FPGAXilinx 3000 and Actel ACT2 family, structured programmable array logic, programming FPGAs, benchmarking of FPGAs.

Unit-IV

Recent developments- new architectures such as Altera FLEX, Pilkington (Motorola/ Toshiba), Xilinx XC4000, field programmable interconnect.

Unit-V

VHDL Synthesis for FPGA Implementation.: Mapping of statements to gateassignment statements, logical, arithmetic and relational operators, vectors and slices, IF, Process, Case, Loop, Null, Wait statements. Modeling of flip-flops and latches. Modeling of FSM for synthesis. Some examples of synthesizable constructs.

Unit-VI

Verilog Synthesis for FPGA Implementation: Verilog constructs and operators, interpretation of Verilog constructs, synthesis design flow- RTL to gates, translation, unoptimized intermediate representations, logic optimization, technology mapping and optimization, technology library, design constraints, optimized gate level description.

TEXT BOOKS:

- 1 S. Palnitkar, *Verilog HDL : A Guide to Digital Design and Synthesis*, PH/Pearson.
- 2 K. Coffman, *Real World FPGA Design with Verilog*, PH.

REFERENCES:

1. P.J. Ashenden, *The Designer's Guide to VHDL*, Second Edition, Morgan Kaufmann.
2. C. H. Roth, *Digital System Design with VHDL*, PWS/Brookscole.
3. R. C. Seals and G. F. Whapshott, *Programmable Logic : PLDs and FPGAs*, MH.
4. A,K. Sharma, *Programmable Logic Handbook : PLDs, CPLDs and FPGAs*, MH.

I Year – I Sem. M.Tech. (DSCE)
CPLD & FPGA ARCHITECTURE AND APPLICATIONS
(ELECTIVE – II)

Code: 5T102

L T P C
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a	b	c	d	e	f	g	h	i	j	k
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After studying this course, the students will be able to

1. Understand the basic architecture of PLDs, CPLDs and the architectures of Max series and Altera Flex series CPLDs.
2. Understand the basic architecture of AMD series, Cypress series, Lattice PLSI CPLDs and their applications.
3. Understand the architectures of Various types of FPGA devices and use it for suitable design examples.
4. Understand the basic concepts of State Machine Charts and petrinet models and also realize the Finite State machines using state machines and petrinets.
5. Understand and explore the design of digital systems using available EDA tools.
6. Understand and analyze some of the case studies of digital system design using EDA tools.

Unit –I

Programmable logic : ROM, PLA, PAL PLD, PGA – Features, programming and applications using complex programmable logic devices Altera series – Max 5000/7000 series and Altera FLEX logic-10000 series CPLD - Speed performance and in system programmability.

Unit –II

Programming and applications using AMD's- CPLD (Mach 1to 5), Cypres FLASH 370 Device technology, Lattice PLST's architectures – 3000 series – Speed performance and in system programmability.

Unit – III

FPGAs: Field Programmable gate arrays- Logic blocks, routing architecture, design flow technology mapping jfor FPGAs, Case studies Xitir x XC4000 & ALTERA's FLEX 8000/10000 FPGAs: AT &T ORCA's (Optimized Reconfigurable Cell Array): ACTEL's ACT-1,2,3 and their speed performance

Unit-IV

Alternative realization for state machine chat using microprogramming linked state machine one –hot state machine, Petri Nets for state machines-basic concepts, properties, and extended Petri Nets for parallel controllers. , Encode State Machines- Traffic Light Controller-Implementation of Petri-net description.

Unit-V

Digital front end digital design tools for FPGAs & ASICs: Using EDA tools – Design flow using FPGAs. Software Tool box - Placement, Routing & wire ability.

Unit - VI

Case studies of parallel adder cell, parallel adder sequential circuits, counters, multiplexers, parallel controllers.

TEXT BOOKS:

1. Field Programmable Gate Array Technology - S. Trimberger, Edr, 1994, Kluwer Academic Publications.
2. Field Programmable Gate Arrays, John V.Oldfield, Richard C Dore, Wiley Publications.
3. Field programmable gate array, S. Brown, R.J.Francis, J.Rose ,Z.G.Vranesic, 2007, BSP.

REFERENCES:

1. Digital Design Using Field Programmable Gate Array, P.K.Chan & S. Mourad, 1994, Prentice Hall.
2. Digital System Design using Programmable Logic Devices – Parag.K.Lala, 2003, BSP.
3. Data Sheets of XILINX & ALTERA
4. Digital Systems Design with FPGA's and CPLDs – Ian Grout, 2009, Elsevier.

I Year -I Sem M.Tech. (DSCE)
INTERNETWORKING
 (ELECTIVE – II)

Code: 5S124

L T P C
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a	b	c	d	e	f	g	h	i	j	k
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After studying this course, the students will be able to

1. Describe Internet working concepts, IP Address and protocols
2. Understand the basic principle and operation of Internet Protocol and Transmission Control Protocol (TCP)
3. Understand the concepts of Stream Control Transmission Protocol, Mobile IP, Classical TCP Improvements.
4. Describe and determine the performance of Unicast and Multicast Routing Protocols.
5. Describe Domain Name System (DNS), TELNET protocols, SNMP and HTTP Architecture.
6. Describes basic principles of Multimedia, compression techniques, security mechanisms, protocols and Voice Over IP.

Unit -I:

Internetworking concepts: Principles of Internetworking, Connectionless Internetworking, Application level Interconnections, Network level Interconnection, Properties of the Internet, Internet Architecture, Wired LANS, Wireless LANS, Point-to-Point WANs, Switched WANs, Connecting Devices, TCP/IP Protocol Suite.

IP Address: Classful Addressing: Introduction, Classful Addressing, Other Issues, Sub-netting and Super-netting

IP Address: Classless Addressing: - Variable length Blocks, Sub-netting, Address Allocation. Delivery, Forwarding, and Routing of IP Packets: Delivery, Forwarding, Routing, Structure of Router.

ARP and RARP: ARP, ARP Package, RARP.

Unit -II:

Internet Protocol (IP): Datagram, Fragmentation, Options, Checksum, IP V.6.

Transmission Control Protocol (TCP): TCP Services, TCP Features, Segment, A TCP Connection, State Transition Diagram, Flow Control, Error Control, Congestion Control, TCP Times.

Unit -III:

Stream Control Transmission Protocol (SCTP): SCTP Services, SCTP Features, Packet Format, Flow Control, Error Control, Congestion Control.

Mobile IP: Addressing, Agents, Three Phases, Inefficiency in Mobile IP.

Classical TCP Improvements: Indirect TCP, Snooping TCP, Mobile TCP, Fast Retransmit/Fast Recovery, Transmission/ Time Out Freezing, Selective Retransmission, Transaction Oriented TCP.

Unit -IV:

Unicast Routing Protocols (RIP, OSPF, and BGP): Intra and Inter-domain Routing, Distance Vector Routing, RIP, Link State Routing, OSPF, Path Vector Routing, BGP.

Multicasting and Multicast Routing Protocols: Unicast - Multicast- Broadcast, Multicast Applications, Multicast Routing, Multicast Link State Routing: MOSPF, Multicast Distance Vector: DVMRP.

Unit -V:

Domain Name System (DNS): Name Space, Domain Name Space, Distribution of Name Space, and DNS in the internet.

Remote Login TELNET:- Concept, Network Virtual Terminal (NVT). *File Transfer FTP and TFTP:* File Transfer Protocol (FTP). *Electronic Mail:* SMTP and POP.

Network Management-SNMP: Concept, Management Components. World Wide Web-HTTP Architecture.

Unit-VI:

Multimedia: Digitizing Audio and Video, Network security, security in the internet firewalls. Audio and Video Compression, Streaming Stored Audio/Video, Streaming Live Audio/Video, Real-Time Interactive Audio/Video, RTP, RTCP, Voice Over IP. Network Security, Security in the Internet, Firewalls.

TEXT BOOKS:

1. TCP/IP Protocol Suite- Behrouz A. Forouzan, Third Edition, TMH
2. Internetworking with TCP/IP Comer 3rd edition PHI

REFERENCES:

1. High performance TCP/IP Networking- Mahbub Hassan, Raj Jain, PHI, 2005
2. Data Communications & Networking – B.A. Forouzan – 2nd Edition – TMH
3. High Speed Networks and Internets- William Stallings, Pearson Education, 2002.
4. Data and Computer Communications, William Stallings, 7th Edition., PEI.

**I Year – I Sem. M.Tech.(DSCE)
DIGITAL CONTROL SYSTEMS
(ELECTIVE – II)**

Code: 122EP21

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X	X	X	X	X	X			X		

After studying this course, the students will be able to

1. Understanding the signal conversion and processing, coding and quantization. Review of transforms
2. Applying transfer functions to digital systems and understanding the closed loop systems, multi rate systems and cyclic rate systems.
3. Understanding the controllability of LTI systems, and also learning how to increase the stability of a system.
4. Learning Time Domain and Z-Domain analysis and applying to the second order systems. Understanding different frequency domain analyses techniques.
5. Designing the discrete data control systems, data controllers and bilinear transformations.
6. Learning the state transition equations, computing the transition matrix and decomposition of discrete systems.

Unit – I

Signal Conversion and Processing

Introduction, Digital Signals and Coding, Data conversion and Quantization, Sample and Hold devices, Analog to Digital conversion, Digital to Analog conversion, Mathematical modeling of the Sampling process, Sampling theorem, Mathematical modeling of Sampling by convolution integral, Flat Top approximation of the finite-pulse width sampling, Data construction and filtering of sampled signals, Zero order hold, first order hold, polygonal hold and slewer hold.

Review of Z-Transform and Applications: Review of Z-Transform, Applications of Z-Transform, Signals between sampling instants – submultiple sampling method & delayed Z-Transform and the Modified Z-Transform.

Unit – II

Transfer Functions, Block Diagrams and Signal Flow Graphs: Introduction, Pulse transfer function and Z-transfer function, Relation between $G(s)$ and $G(z)$, Closed loop systems, sampled signal flow graph, Modified Z-transfer function, Multirate discrete data systems (slow-fast, fast-slow, Multirate systems with all digital systems, Closed loop multi sampled systems, and cyclic rate sampled systems.

Unit – III

Controllability, Observability and Stability: Introduction, Controllability of Linear time invariant discrete data systems, Observability of Linear time invariant discrete data systems, Relationships between Controllability, Observability and Transfer Functions, Stability of

Linear Digital Control Systems, Stability tests of discrete data systems (bilinear transformation method – Extension of RH criterion, Jury's stability test).

Unit – IV

Time Domain and Z-Domain Analysis: Introduction, prototype second order system, comparison of time responses of continuous data and discrete data systems, steady state error analysis of digital control systems, correlation between time response and root locations in S-plane and Z-plane, Dominant characteristic equation, Root loci of digital control systems, Effects of adding poles and zeroes to open loop transfer function.

Frequency Domain Analysis: Introduction, Polar plot of $GH(z)$, Nyquist stability criterion, Bode plot, Gain margin and Phase margin, Bandwidth considerations and Sensitivity analysis.

Unit-V

Design of Discrete Data Control Systems: Introduction, Cascade compensation by continuous data controllers, Design of continuous data controllers with equivalent digital controllers, Digital Controllers, Design of digital control systems with digital controllers and bilinear transformation.

Unit – VI

State Variable Technique: State equations of discrete data systems with sample and hold devices, State equations of digital systems with all digital elements, State transition equations (recursive method and Z-transform method), Relationship between State equations and Transfer Functions, Characteristic equation, Eigen values and Eigen vectors, Methods of computing the Transition Matrix (Cayley Hamilton theorem, Z-transform method), State diagrams of digital systems, De-composition of discrete data transfer functions.

TEXT BOOKS: 1. Digital Control Systems - Kuo, Oxford, 2nd Edition.

REFERENCES:

1. Discrete-Time Control Systems - Katsuhiko Ogata, 2nd Edition, PHI
2. Digital Control and State Variable Methods (Conventional and Intelligent Control Systems) by M.Gopal, 3rd edition, TMH

I Year – I Sem. M.Tech.(DSCE)
Embedded Control System
(ELECTIVE – II)

Code: 5T110

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After studying this course, the students will be able to

1. Understanding the signal conversion and processing, coding and quantization. Review of transforms
2. Applying transfer functions to digital systems and understanding the closed loop systems, multi rate systems and cyclic rate systems.
3. Understanding the controllability of LTI systems, and also learning how to increase the stability of a system.
4. Learning Time Domain and Z-Domain analysis and applying to the second order systems. Understanding different frequency domain analyses techniques.
5. Designing the discrete data control systems, data controllers and bilinear transformations.
6. Learning the state transition equations, computing the transition matrix and decomposition of discrete systems.

Unit-I

INTRODUCTION Controlling the hardware with software – Data lines, Address lines, Ports – Schematic representation – Bit masking – Programmable peripheral interface – Switch input detection – 74 LS 244

Unit-II

INPUT-OUTPUT DEVICES Keyboard basics – Keyboard scanning algorithm – Multiplexed LED displays – Character LCD modules, LCD module display, Configuration – Time-of-day clock – Timer manager – Interrupts – Interrupt service routines, IRQ, ISR, Interrupt vector or dispatch table multiple-point – Interruptdriven pulse width modulation.

Unit- III

D/A AND A/D CONVERSION R 2R ladder – Resistor network analysis – Port offsets – Triangle waves analog vs. digital values – ADC0809 – Auto port detect – Recording and playing back voice – Capturing analog information in the timer interrupt service routine – Automatic, multiple channel analog to digital data acquisition.

Unit-IV

ASYNCHRONOUS SERIAL COMMUNICATION Asynchronous serial communication – RS-232, RS-485 – Sending and receiving data – Serial ports on PC – Low-level PC serial I/O module, Buffered serial I/O.

Unit-V

CASE STUDIES: EMBEDDED C PROGRAMMING Multiple closure problems – Basic outputs with PPI

Unit-VI

Controlling motors – Bi-directional control of motors – H bridge – Telephonic systems – Stepper control – Inventory control systems.

REFERENCE BOOKS:

1. Jean J. Labrosse, "Embedded Systems Building Blocks: Complete and Ready-To-Use Modules in C", The publisher, Paul Temme, 2003.
2. Ball S.R., „Embedded microprocessor Systems – Real World Design“, Prentice Hall, 2001.
3. Herma K, "Real Time Systems – Design for distributed Embedded Applications", Kluwer Academic, 2003.
4. Daniel W. Lewis, "Fundamentals of Embedded Software where C and Assembly meet", PHI, 2002.

I Year – I Sem. M.Tech.(DSCE)
Embedded System for Wireless & Mobile Communication
(ELECTIVE-II)

Code : 5U106

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3 1 - 3

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X	X	X	X	X						

After going through the course, the student will be able to

1. Understanding the signal conversion and processing, coding and quantization. Review of transforms
2. Applying transfer functions to digital systems and understanding the closed loop systems, multi rate systems and cyclic rate systems.
3. Understanding the controllability of LTI systems, and also learning how to increase the stability of a system.
4. Learning Time Domain and Z-Domain analysis and applying to the second order systems. Understanding different frequency domain analyses techniques.
5. Designing the discrete data control systems, data controllers and bilinear transformations.
6. Learning the state transition equations, computing the transition matrix and decomposition of discrete systems.

Unit-I

Introduction to wireless technologies: WAP services, Serial and Parallel Communication, Asynchronous and synchronous Communication, FDM,TDM, TFM, Spread spectrum technology

Unit-II

Introduction to Bluetooth: Specification, Core protocols, Cable replacement protocol
 Bluetooth Radio: Type of Antenna, Antenna Parameters, Frequency hopping Bluetooth
 Networking: Wireless networking, wireless network types, devices roles and states, adhoc network, scatter net

Unit-III

Connection establishment procedure, notable aspects of connection establishment, Mode of connection.

Unit-IV

Bluetooth security, Security architecture, Security level of services, Profile and usage model: Generic access profile (GAP), SDA, Serial port profile, Secondary bluetooth profile

Unit-V

Hardware: Bluetooth Implementation, Baseband overview, packet format, Transmission buffers, Protocol Implementation: Link Manager Protocol, Logical Link Control adaptation Protocol, Host control Interface, Protocol Interaction with layers

Unit-VI

Programming with Java: Java Programming, J2ME architecture, Javax. bluetooth package Interface, classes, exceptions, Javax. obex Package: interfaces, classes Bluetooth services registration and search application, bluetooth client and server application.
Overview of IrDA, HomeRF, Wireless LANs, JINI

TEXT BOOKS:

1. Bluetooth Technology by C.S.R. Prabhu and A.P. Reddi; PHI
2. Wireless communication by Rappaport
3. Mobile communication by Schiller
4. Mobile communication by C.Y.Lee

I Year – I Sem. M.Tech.(DSCE)
CAD FOR VLSI CIRCUITS
(ELECTIVE – II)

Code: 5T111

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After studying this course, the students will be able to

1. *Learn VLSI Design Methodologies, Data structures and Design Automation Tools.*
2. *Learn the Algorithmic Graph theory and Computational complexity, general purpose methods for combinatorial optimization.*
3. *Learn various Design Rules, Layout Compaction, algorithms for constraint graph compaction, and placement and partitioning.*
4. *Understand floor planning concepts, shape functions and floor plan sizing, and types of local routing problems.*
5. *Understand Simulation, gate level modeling and simulation, switch level modeling and simulation, and combinational logic synthesis.*
6. *Learn modeling and synthesis, high level synthesis, assignment and scheduling etc.*

Unit I

VLSI DESIGN METHODOLOGIES

Introduction to VLSI Design methodologies - Review of Data structures and algorithms - Review of VLSI Design automation tools
Applications- high-performance computing, telecommunications, and consumer electronics

Unit II

Algorithmic Graph Theory and Computational Complexity - Tractable and Intractable problems - general purpose methods for combinatorial optimization.
Applications- computations, operations research, and molecular biology.

Unit III

DESIGN RULES

Layout Compaction - Design rules - problem formulation - algorithms for constraint graph compaction - placement and partitioning - Circuit representation - Placement algorithms – partitioning
Applications - CMOS fabrication process

Unit IV

FLOOR PLANNING

Floor planning concepts - shape functions and floorplan sizing - Types of local routing problems - Area routing - channel routing - global routing - algorithms for global routing.
Applications – EDA tools

Unit V

SIMULATION

Simulation - Gate-level modeling and simulation - Switch-level modeling and simulation - Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis.
Applications – circuit design and analogue and mixed-signal IC design

Unit VI

MODELING AND SYNTHESIS

High level Synthesis - Hardware models - Internal representation - Allocation - assignment and scheduling - Simple scheduling algorithm - Assignment problem - High level transformations.

Application - Electronic VLSI Design Tools(EDA Tools).

REFERENCES

1. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons, 2002.
2. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002.

**I Year – II Sem. M.Tech.(DSCE)
TESTING OF VLSI CIRCUITS
(ELECTIVE-II)**

Code: 5T204

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After studying this course, the students will be able to

1. *Understand the important of testing, types of testing*
2. *Explore the various types of faults and fault models in VLSI circuits.*
3. *Understand the various algorithms of fault simulation.*
4. *Understand and explore the concept of Testability and its measure.*
5. *Demonstrate the BIST process for logic testing, memory testing and delay fault testing.*
6. *Be familiar with Boundary Scan Test and Boundary scan instructions .*

Unit-I**INTRODUCTION TO TESTING:**

Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Test economics, Yield, Defect level as a Quality Measures.

Unit-II**FAULT MODELING:**

Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT III**LOGIC AND FAULT SIMULATION:**

Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation, ATPG.

UNIT IV**TESTABILITY MEASURES:**

SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT V**BUILT-IN SELF-TEST:**

The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

UNIT VI

BOUNDARY SCAN STANDARD

TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BSDL Description Components, Pin Descriptions.

TEXT BOOKS:

1. Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits - M.L. Bushnell, V. D. Agrawal, Kluwer Academic Publishers

REFERENCES:

1. Digital Systems and Testable Design - M. Abramovici, M.A.Breuer and A.D Friedman, Jaico Publishing House.
2. Digital Circuits Testing and Testability - P.K. Lala, Academic Press.

**I Year – II Sem. M.Tech.(DSCE)
RESEARCH METHODOLOGY**

Code: 5S125

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1 1 - 1

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After completing the course students are able to understand

1. Study the concepts of Research, Characteristics and Prerequisites of research, Research needs in Engineering, Education, Science and Management .
2. Study the concepts of Conducting a literature search, Evaluating, Organizing, and synthesizing the literature.
3. Identifying and describing the research, finding the research Problem, Sources of research problem
4. Perform Quantitative / Qualitative Research Design
5. Familiar with concept of Formatting a research proposal.
6. Familiar with writing Research report

Unit- I

What is Research? What is not Research? Meaning, aim, nature and scope of research, Characteristics and Prerequisites of research, Research needs in Engineering, Education, Science and Management, Research benefits to Society in general.

Unit II

Role of Review, Search for related literature, On line search, Searching Web, Conducting a literature search, Evaluating, Organizing, and synthesizing the literature.

Unit- III

Identifying and describing the research ,Finding the research Problem, Sources of research problem, Criteria/ Characteristics of a Good research.

Unit – IV

The Nature and role of Data in Research, Linking Data and Research Methodology, Validity of Method, Planning for Data collection, Choosing a Research Approach, Use of Quantitative / Qualitative Research Design, Feasibility of Research Design, Establishing Research Criteria, Justification of Research Methodology.

Unit- V

Characteristics of a proposal, Formatting a research proposal, Preparation of proposal, Importance of Interpretation of data and treatment of data.

Unit- VI

Format of the Research report, Style of writing report, References and Bibliography.

REFERENCES

1. Practical Research : planning and Design(8th Edition) – Paul D. Leedy and Jeanne E. Ormrod.
2. [www. Prenhall.com/leedy](http://www.Prenhall.com/leedy).
3. A Hand Book of Education Research – NCTE
4. Methodogy of Education Research – K.S. Sidhu.
5. Research Methodology. Methods & Technique : Kothari. C.R.
6. Tests, Measurements and Research methods in Behavioural Sciences- A.K. Singh.
7. Statistical Methods- Y.P. Agarwal.
8. Methods of Statistical Ananalysis- P.S Grewal.
9. Fundamentals of Statistics – S.C. Gupta, V.K. Kapoor.

**I Year -I Sem M.Tech. (DSCE)
SIMULATION LAB (VHDL / Verilog)**

Code : 5U171

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After going through the Laboratory course, the student will be able to

1. Design, Simulate, Verify, Synthesize Various Logic gates and also implement them on SPARTAN3 FPGA IC.
2. Design, Simulate, Verify and Synthesize Various Logic Blocks which perform Arithmetical, logical and relational Operations on Digital Data using all Modeling styles and also implements them on SPARTAN3 FPGA IC.
3. Design, Simulate, Verify and synthesize various combinational Blocks or circuits using all modelling styles and Also implement them on SPARTAN3 FPGA IC.
4. Design, Simulate, Verify and Synthesize Various Sequential Blocks or circuits using all modelling styles and also implement them on SPARTAN3 FPGA IC.
5. Verify the functionality using functional simulator, calculate critical path using timing simulator and perform placement, routing and implementation on SPARTAN3 FPGA IC.

Design of Experiments:

Statistical methods, Randomised block design, Latin and orthogonal squares, factorial design, Replication and randomization.

Data Analysis: Deterministic and random data, uncertainty analysis, tests for significance: Chi-square, student's 't' test, regression modeling, direct and interaction effects, ANOVA, F-test, Time series analysis, Autocorrelation and autoregressive modeling.

Text Book:

1. "The Design and Analysis of industrial Experiments", Davis. O. V.; Longman, London.

LIST OF EXPERIMENTS:

CYCLE 1:

1. Simulation and Verification of Logic Gates.
2. Design and Simulation of adder, Serial Binary Adder, Multi Precession Adder, Carry Look Ahead Adder.
3. Simulation and verification of Decoder, MUXs, Encoder using all Modeling Styles.
4. Modeling of Flip-Flops with Synchronous and Asynchronous reset.
5. Design and simulation of Counters- Ring Counter, Johnson Counter, Up- Down Counter, Ripple Counter.
6. Design of a N- bit Register of Serial- in Serial –out, Serial in parallel out, Parallel in Serial out and Parallel in Parallel Out.
7. Design of Sequence Detector (Finite State Machine- Mealy and Moore Machines).

8. 4- Bit Multiplier, Divider.
9. ALU to Perform – ADD, SUB, AND-OR, 1'S AND 2'S COMPLEMENT, Multiplication, Division.

CYCLE 2: After Digital Circuit Description Using Verilog/ VHDL.

1. Verification of the Functionality of the circuit using function Simulators.
2. Timing Simulator for Critical Path time Calculation.
3. Synthesis of Digital Circuit.
4. Place and Router Techniques for FPGA's like Xilinx, Altera, Cypress, etc.,
5. Implementation of Design using FPGA and CPLD Devices.

**I Year -I Sem M.Tech. (DSCE)
LITERATURE REVIEW SEMINAR - 1**

Code: 5U172

L	T	P	C
-	-	3	1

Max. Marks: 100

a	b	c	d	e	f	g	h	i	j	k
X	X		X				X	X		

After studying this course, the students will be able to

1. Identify a research topic
2. Collect literature
3. Present seminar
4. Discuss the queries

There shall be three seminar presentations during I year I semester and I year II Semester. For seminar, a student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the Department in a report form and shall make an oral presentation before the Departmental Committee, which shall consist of the Head of the Department, a senior Faculty Member and the Supervisor and will jointly evaluate the report and presentation. For each Seminar there will be only internal evaluation of 25 marks. A candidate has to secure a minimum of 50% to be declared successful.

In the First semester the report must be in the form of the review paper with a format used by IEEE / ASME etc. In the Second semester Technical Seminar in the form of Independent Review Paper must be of high quality fit for publication in a reputed conference / journal.

The evaluation format for seminar is as follows:

- Day to day evaluation by the Supervisor : 5 marks
- Final Report : 5 marks
- Presentation : 15 marks

A Student has to concentrate on the following sections while writing technical paper or presenting seminar.

Contents:

- Identification of specific topic
- Analysis
- Organization of modules

- Naming Conventions
- Writing style
- Figures
- Feedback
- Writing style
- Rejection
- Miscellaneous

REFERENCES:

Teach Technical Writing in Two Hours per Week by Norman Ramsey

For Technical Seminar the student must learn few tips from sample seminars and correcting himself, which is continues learning process

REFERENCE LINKS:

1. <http://www.cs.dartmouth.edu/~scot/givingTalks/sld001.htm>
2. <http://www.cse.psu.edu/~yuanxie/advice.htm>
3. <http://www.eng.unt.edu/ian/guides/postscript/speaker.pdf>

NOTE: A student can use any references for this process, but must be shared in classroom.

**I Year – I Sem. M.Tech.(VLSI & Embedded Systems)
COMPREHENSIVE VIVA-VOCE - 1**

Code: 5U174

L T P C
- - - 1

Max. Marks: 100

a	b	c	d	e	f	g	h	i	j	k
X	X						X	X		X

There shall be a Comprehensive Viva-Voce in II year I Semester. The Comprehensive Viva-Voce will be conducted by a Committee consisting of Head of the Department and two Senior Faculty members of the Department. The Comprehensive Viva-Voce is aimed to assess the students' understanding in various subjects he/she studied during the M.Tech course of study. The Comprehensive Viva-Voce is valued for 50 marks by the Committee. There are no internal marks for the Comprehensive Viva-Voce. A candidate has to secure a minimum of 50% to be declared successful.

**I Year – II Sem. M.Tech.(DSCE)
ADVANCED COMPUTER ARCHITECTURE**

Code: 5S223

L T P C
3 1 - 3

a	b	c	d	e	f	g	h	i	j	k
X	X	X	X	X	X					

After studying this course, the students will be able to

1. Describe various instruction formats and addressing modes, instruction set of a computer, instruction cycle.
2. Describe processor organization, register organization and stack organization. Describe power PC processor and Pentium processor, RISC and CISC instruction set.
3. Describe various memories organizations.
4. Compare and contrast program driven, interrupt driven, direct memory access, input and output mechanisms.
5. Explain Horizontal and vertical instruction format, instruction pipelining, parallel processing and hazards.
6. Describe hardware and software solutions for ILP. RAID levels, Design of an I/O system and describe practical issues in interconnecting networks and design cluster

Unit I

Concept of instruction format and instruction set of a computer, types of operands and operations; addressing modes, processor organization, register organization and stack organization; instruction cycle, basic details of Pentium processor and Power PC processor, RISC and CISC instruction set.

Unit II

Memory devices; Semiconductor and Ferrite core memory, main memory, cache memory, associative memory organization, concept of virtual memory, memory organization and mapping, partitioning, demand paging, segmentation, magnetic disk organization, introduction to magnetic tape and CDROM.

Unit III

IO Devices, Programmed IO, interrupt driver IO, DMA IO modules, IO addressing, IO channel, IO processor, DOT matrix printer, inkjet printer, laser printer.
Advanced concepts: Horizontal and Vertical instruction format, microprogramming, microinstruction sequencing and control, instruction pipeline, parallel processing, problems in parallel processing, data hazard, control hazard.

Unit IV

ILP software approach- compiler techniques- static branch protection- VLIW approach- H.W support for more ILP at compile time- H.W verses S.W solutions
Multiprocessors and thread level parallelism- symmetric shared memory architectures- distributed shared memory- Synchronization- multi threading.

Unit V

Storage systems- Types – Buses - RAID- errors and failures- bench marking a storage device- designing a I/O system.

Unit VI

Inter connection networks and clusters- interconnection network media – practical issues in interconnecting networks- examples – clusters- designing a cluster

TEXT BOOKS

1. Computer Organization and Architecture – William Stallings, PHI, 1998.
2. Computer Organization – Carl Hamachar, Zvonko Vranesic, Safwat Zaky, McGraw Hill International.
3. Computer Achitecture & Organization – John P. Heyes, TMH, 3rd edition.
4. Computer Architecture - A quantitative approach; 3rd edition, John L. Hennessy & David A. Patterson, Morgan Kufmann (An Imprint of Elsevier)

REFERENCE BOOKS

1. Computer Architecture and parallel Processing - Kai Hwang and A.Briggs, McGraw-Hill.
2. Advanced Computer Architectures, Dezso Sima, Terence Fountain, Peter Kacsuk, Pearson.

**I Year – I Sem. M.Tech.(DSCE)
LOW POWER VLSI DESIGN**

Code: 5T106

L T P C
3 1 - 3

a	b	c	d	e	f	g	h	i	j	k
X	X	X	X	X	X	X				X

After going through the course, the student will be able to

1. Understand the implications of Low Power Design on IC Fabrication.
2. Understand the various deep submicron Processes and their future trends and directions.
3. Understand and analyse various MOSFET and Bipolar models and their limitations.
4. Know, Understand the conventional CMOS and BiCMOS logic gates, able to analyse power dissipation of the CMOS Inverter and its implementation of two- i/p NOR and NAND gates. He is also able to understand the basic driver configurations of the BiCMOS logic gate associated with shunting devices for full o/p voltage swing.
5. Understand the design of various low power BiCMOS circuits for high performance at low power supply voltages.
6. Trace out the reasons for Evolution of Latches and Flip flops. He is also able to understand the quality measures for latches and Flip flops and Design perspective.

Unit I

INTRODUCTION: low power design - an over view, Low-Voltage, Low power design limitations, Silicon-on-Insulator Technology.

MOS/BICMOS PROCESSES-TECHNOLOGY AND INTEGRATION: Introduction, The realization of BiCMOS processes-Low cost medium speed 5volts digital BiCMOS process, High performance high cost 5volts digital BiCMOS process, Twin well BiCMOS process; BiCMOS manufacturing and Integration considerations-Consideration for CMOS device structures, Process consideration for Bipolar transistors; Isolation in BiCMOS- Isolation in Bipolar transistors, Isolation in MOS transistors; Advanced isolation technologies.

Unit II

DEEP SUBMICRON PROCESSES: Polysilicon Emitter High-Performance BiCMOS Structure, Low capacitance Bipolar/BiCMOS Processes,SOI CMOS/BiCMOS VLSIs.

LOW-VOLTAGE/LOW POWER CMOS/ BICMOS PROCESSES: Low Voltage/Low Power SOI CMOS, Properties of fully depleted SOI MOSFETs, Low Voltage/Low Power Lateral BJT on SOI, Future trends and Directions of CMOS/BiCMOS processes.

Unit III

CMOS AND Bi-CMOS LOGIC GATES: Conventional CMOS logic gates.

CONVENTIONAL BICMOS LOGIC GATES:Basic Driver configurations, Full swing with shunting devices, FS-CMBL, FS-CMBL with feedback, High performance CCBiCMOS circuit.

Unit IV

LOW- VOLTAGE LOW POWER LOGIC CIRCUITS-1: BiCMOS Circuits Utilizing Lateral pnp BJTs in pMOS Structures, Merged BiCMOS Digital Circuits, Full-Swing Multi Drain/Multi Collector Complementary BiCMOS Buffers, Qasi Complementary BiCMOS Digital Circuits, Full-Swing BiCMOS/BiNMOS Digital Circuits Employing Schottky Diodes.

Unit V

LOW- VOLTAGE LOW POWER LOGIC CIRCUITS-2: Feedback type BiCMOS Digital Circuits, High-Beta BiCMOS Digital Circuits, Transiently Saturated Full-Swing BiCMOS Digital Circuits, Bootstrapped-Type BiCMOS Digital Circuits-1.5volts Bootstrapped BiCMOS logic gate, Bootstrapped FS BiCMOS/BiNMOS Inverter, ESD-free Bi CMOS Digital Circuit.

Unit VI

LOW POWER LATCHES AND FLIP FLOPS: Evolution of Latches and Flip flops-The Functionality Theme, The Synchronous Theme, The Optimization Theme, The Performance Theme, The Pipelining Theme, The high performance and low power theme;

QUALITY MEASURES FOR LATCHES AND FLIP FLOPS: Performance Measures, Power dissipation measures, Area measures.

TEXT BOOKS

1. CMOS/BiCMOS ULSI low voltage, low power by Yeo Rofail/ Gohl(3 Authors)- Pearson Education Asia 1st Indian reprint,2002

REFERENCES

1. Digital Integrated circuits , J.Rabaey PH. N.J 1996
2. CMOS Digital ICs , Sung-moKang and Yusuf Leblebici 3rd edition TMH 2003 (chapter 11)
3. VLSI DSP systems , Parhi, John Wiley & sons, 2003 (chapter 17)
4. IEEE Trans Electron Devices, IEEE J.Solid State Circuits, and other National and International Conferences and Symposia

**I Year – II Sem. M.Tech.(DSCE)
DESIGN OF FAULT TOLERANT SYSTEMS**

Code: 5U201

L T P C
3 1 - 3

a	b	c	d	e	f	g	h	i	j	k
x	X		X	X				X		

After going through the course, the student will be able to

1. Understand the concepts of reliability and other related terms and fault tolerance using different types of redundancy techniques.
2. Explore the concepts of fault checking circuits using totally self checking circuits, Berger code and residue codes. Also Design fault safe circuits using partition theory and Berger Code.
3. Understand and explore the test pattern generation using ATPG process for transition delay and path delay faults.
4. Understand and analyze various design for testability techniques such as Reed Muller's expansion technique, OR-AND-OR design etc.
5. Understand the methods of sequential circuit testing using scan architecture, Boundary scan test, multiple sanchains, LSSD and at-speed testing.
6. Understand and design the Built-in Self Test techniques and test pattern generation methods for regular and irregular design arrays.

Unit I

BASIC CONCEPTS: Reliability concepts, Failure & Faults, Reliability and failure rate, Relation between reliability and Meantime between failure, Maintainability and Availability, Reliability of series, Parallel and Parallel-Series combinational circuits.

FAULT TOLERANT DESIGN: Basic concepts – Static, dynamic, hybrid, Triple Modular Redundant System, Self purging redundancy, Siftout redundancy (SMR), 5 MR re-configuration techniques, Use of error correcting code, Time redundancy and software redundancy.

Unit II

SELF CHECKING CIRCUITS: Basic concepts of Self checking circuits, Design of Totally Self Checking checker, Checkers using m out of n codes, Berger code, Low cost residue code.

FAIL SAFE DESIGN: Strongly fault secure circuits, fail safe design of sequential circuits using partition theory and Berger code, Totally self checking PLA design.

Unit III

Introduction to ATPG, ATPG process – Testability and Fault Analysis methods, Fault masking, Transition delay fault ATPG, Path delay, fault ATPG.

Unit IV

DESIGN FOR TESTABILITY FOR COMBINATIONAL CIRCUITS: Basic concepts of testability, controllability and observability, the Reed Muller's expansion technique, OR-AND-OR design, use of control and syndrome testable designs.

Unit V

Scan Architectures and Techniques: Introduction to scan based testing, functional testing, the scan effective circuit, the MUX-D style scan flip-flops, the scan shift register, scan cell operation.

Scan Test Sequencing, scan test timing, partial scan, multiple scan chains, scan based design rules (LSSD), At-speed scan testing and architecture, multiple clock and scan domain operation, critical paths for At-speed scan test. Boundary Scan Test: JTAG Test Operations

Unit VI

BUILT IN SELF TEST (BIST): BIST concepts, Test pattern generation for BIST exhaustive testing, Pseudorandom testing, pseudo exhaustive testing, constant weight patterns, Generic offline BIST architecture, memory test architecture.

TEXT BOOKS:

1. Fault Tolerant & Fault Testable Hardware Design - Parag K. Lala, PHI
2. Design for Test for Digital ICs and Embedded Core Systems – Alfred L. Crouch, 2008, Pearson Education.
3. Fundamentals of Logic Design – Charles H. Roth, 5th ed., Cengage Learning.

REFERENCES:

1. Digital Systems Testing and Testable Design - M. Abramovili, M.A. Breues, A. D. Friedman, Jaico publications.
2. Essentials of Electronic Testing – Bushnell, and Vishwani D. Agarwal, Springers.

I Year – II Sem. M.Tech.(DSCE)
EMBEDDED REAL TIME OPERATING SYSTEMS

Code: 5T202

L T P C
3 1 - 3

a	b	c	d	e	f	g	h	i	j	k
X	X	X	X	X	X	X		X		X

After going through the course, the student will be able to

- 1: Understand embedded systems and various options and challenges in building them.*
- 2. Understand the Real Time Systems and various parameters of tasks and models.*
- 3. Understand various scheduling policies.*
- 4. Understand the constructs used for inter-process communication.*
- 5. Understand various services provided RTOS and Micro C/O.S.-II.*
- 6.Understand Vx WORKS O.S. and some case studies*

Unit I: Introduction

Embedded systems overview, design challenges, processor technology, I.C. technology, design technology, trade-offs. Single purpose processors, optimizing custom single purpose processors and general purpose processors, ASIPS, microcontrollers and DSP processors for embedded systems.

Unit II: Real Time Systems:

Typical real time applications, Hard Vs Soft real-time systems, A reference model of Real Time Systems: Processors and Resources, Temporal Parameters of real Time Work load, Periodic task model precedence constraints and data dependency, functional parameters, Resource Parameters of jobs and parameters of resources.

Unit III: Scheduling

Commonly used Approaches to Real Time Scheduling Clock Driven, Weighted Round Robin, Priority Driven, Dynamic Vs State Systems, Effective release time and Dead lines, Offline Vs Online Scheduling. Scheduling real time tasks in multi processor and distributed systems.

Unit IV: Inter-process Communication

Inter-process Communication and Synchronization of Processes, Tasks and Threads- Multiple Process in an Application, Problem of Sharing data by multiple tasks & routines, Inter-process communication

Unit V: Real Time Operating Systems & Programming Tools

Operating Systems Services, I/O Subsystems, RT & Embedded Systems OS, Interrupt Routine in RTOS

Environment

Micro C/OS-II- Need of a well Tested & Debugged RTOs, Use of μ COS-II

Unit VI: VX Works & Case Studies

Memory managements task state transition diagram, pre-emptive priority, Scheduling context switches- semaphore- Binary mutex, counting watch dugs, I/O system

Case Studies of programming with RTOS- Case Study of Automatic Chocolate Vending m/c using μ COS RTOS, case study of sending application Layer byte Streams on a TCP/IP network, Case Study of an Embedded System for a smart card.

TEXT BOOKS:

1. Embedded Systems- Architecture, Programming and Design by Rajkamal, 2nd ed., 2008, TMH.
2. Real Time Systems- Jane W. S. Liu- PHI.
3. Real Time Systems- C.M.Krishna, KANG G. Shin, 1996, TMH
4. Embedded system Design-A unified hardware/ software approach by Frank Vahid, Tony D. Givargis, Johnwiley, 2002.

REFERENCES:

1. Advanced UNIX Programming, Richard Stevens
2. VX Works Programmers Guide

I Year – II Sem. M.Tech. (DSCE)
ENTREPRENEURSHIP AND INNOVATION
(OPEN ELECTIVE)

Code: 5ZC47

L T P C
3 1 - 3

a	b	c	d	e	f	g	h	i	j	k
X					X	X		X		X

After studying this course, the students will be able to

- 1: Acquire qualities of an Entrepreneur
- 2: Understand how to set up an organization
- 3: Carry out SWOT analysis for setting up small business unit
- 4: Acquire decision making managerial behavior
- 5: Develop knowledge on getting financial support from various funding agencies
- 6: Buildup strategies for a successful business

The objective of the course is to make students understand the nature of entrepreneurship, and to motivate the student to start his/her own enterprise with innovative skills.

Unit 1: Nature of Entrepreneurship; Characteristics, Qualities and skills of an Entrepreneur, functions of entrepreneur, Entrepreneur scenario in India and Abroad. Forms of Entrepreneurship: Small Business, Importance in Indian Economy, Types of ownership, sole trading, partnership, Joint Stock Company and other forms. First-Mover disadvantages, Risk Reduction strategies, Market scope strategy, Imitation strategies, and Managing Newness.

Unit 2: Aspects of Promotion: Generation of new entry opportunity, SWOT Analysis, Technological Competitiveness, legal regulatory systems, patents and trademarks, Intellectual Property Rights- Project Planning and Feasibility Studies- Major steps in product development.

Unit 3: MANAGEMENT OF SMALL BUSINESS:

Pre feasibility study - Ownership - budgeting - project profile preparation - Feasibility Report preparation - Evaluation Criteria- Market and channel selection- Product launching - Monitoring and Evaluation of Business- Effective Management of Small business.

Unit 4: SUPPORT SYSTEMS FOR ENTREPRENEURS:

Institutional Support, Training institution, Financial Institutions and Aspects: Sources of raising Capital, Debt-Equity, Financing by Commercial Banks, Government Grants and Subsidies, Entrepreneurship Promotion Schemes of Department of Industries (DIC), KVIC, SIDBI, NABARD, NSIC, APSFC, IFCI and IDBI. New Financial Instruments. Research and Development – Marketing and legal aspects, Taxation benefits, Global aspects of Entrepreneurship.

Unit 5: INTRODUCTION TO INNOVATION:

Meaning of innovation, sources of innovative opportunity, 7 sources of innovative opportunity, Principles of innovation, the enablers of innovation, business insights, insights for innovation, technical architecture for innovation, focus on the essence of innovation.

Unit 6: PROCESS AND STRATEGIES FOR INNOVATION:

Process of innovation, the need for a conceptual approach, Factors contributing to successful technological innovation, Strategies that aim at innovation, impediments to value creation and innovation.

Text Books:

1. Robert D Hisrich, Michael P Peters, Dean A Shepherd: Entrepreneurship, TMH, 2009
2. H. Nandan: Fundamentals of Entrepreneurship, PHI, 2009.

References:

1. Bholanath Dutta: Entrepreneurship – Text and cases, Excel, 2009.
2. Vasanth Desai: Entrepreneurship, HPH, 2009
3. Barringer: Entrepreneurship, Pearson,2009.
4. Peter Drucker (1993), “Innovation and Entrepreneurship”, Hyper Business Book.
5. C.K. Prahalad, M.S. Krishnan, The new age of Innovation – Tata McGraw-Hill, Edition 2008

I Year – II Sem. M.Tech.(DSCE)
SYSTEM-ON-CHIP ARCHITECTURE
(ELECTIVE III)

Code: 5T204

L **T** **P** **C**
3 **1** **-** **3**

a	b	c	d	e	f	g	h	i	j	k
X	X	X	X	X	X					X

After completing the course students are able to understand

- 1.Understanding the abstraction in the hardware design. Learning the processor design and trade offs
- 2.Learning the architecture of ARM processor, execution of instructions
- 3.Learning how to programme a RAM processor with Architecture
- 4.Understanding the Memory concepts.
- 5.Understanding the structural support for the System Management.
- 6.Understanding the concepts of Operating systems.

Unit I:

Introduction to processor design: Abstraction in hardware design, MUO a simple processor, Processor design trade off, design for low power consumption.

Unit II:

ARM Processor as System-on-Chip: Acorn RISC machine – Architecture inheritance – ARM programming model – ARM development tools – 3 and 5 stage pipeline ARM organization – ARM instruction execution and implementation – ARM coprocessor interface.

Unit III:

ARM assembly language programming: ARM instruction types – data transfer, data processing and control flow instructions – ARM instruction set – Coprocessor instructions.
Architectural support for high level language: Data types – abstraction in software design – Expressions – Loops – Functions and Procedures – Conditional statements – use of memory.

Unit IV:

Memory Hierarchy: Memory size and speed – on chip memory – caches – cache design - an example – memory management.

Unit V:

Architectural support for System Management: Advanced microcontroller bus architecture – ARM memory interface – ARM reference peripheral specification – Hardware system prototyping tools – Armulator – Debug architecture.

Unit VI:

Architectural support for Operating System: An introduction to Operating Systems – ARM system control coprocessor – CP15 protection unit registers – ARM protection unit – CP15 MMU registers – ARM MMU architecture – Synchronization – Context switching input and output.

TEXT BOOKS

1. ARM System on Chip Architecture, Steve Furber, 2nd ed. 2000, Addison Wesley Professional.
2. Design of System on a Chip: Devices and Components, Ricardo Reis, 1st ed. 2004, Springer.

REFERENCE BOOKS

1. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology), Jason Andrews, Newnes, BK and CDROM.
2. System on Chip Verification: Methodologies and Techniques, Prakash Rasnikar, Peter Paterson and Leena Singh. L, 2001, Kluwer Academic Publisher.

I Year – II Sem. M.Tech.(DSCE)
CMOS ANALOG & MIXED SIGNAL DESIGN
(ELECTIVE III)

Code: 5U202

L T P C
3 1 - 3

a	b	c	d	e	f	g	h	i	j	k
X	X		X							

After completing the course students are able to understand

1. *Understanding basic circuit connections, functionality and their objectives. Learning the procedures involved in Current Mirror, matching in MOSFET mirrors. Voltage dividers, band gap voltage references, referenced Self-biasing.*
2. *Understanding the design and functioning of Amplifiers and Feedback Amplifiers and their stability.*
3. *Understanding the design and functioning of different types of Differential Amplifiers and their merits and demerits.*
4. *Understanding the design and functioning of Operational Amplifiers like basic CMOS Op-Amp, OTA.*
5. *Learning the Non-Linear & Dynamic Analog Circuits and their designing and Applications.*
6. *Learning the Data Converter Fundamentals, DAC & ADC specifications, Mixed Signal Layout issues, DAC architectures, ADC architectures*

I. CMOS ANALOG CIRCUITS:**Unit I****CURRENT SOURCES, SINKS & REFERENCES**

The cascode connection, sensitivity and temperature analysis, transient response, layout of simple Current Mirror, matching in MOSFET mirrors, other Current Sources/Sinks. Voltage dividers, current source self-biasing.

Unit II**AMPLIFIERS & FEEDBACK AMPLIFIERS**

Gate Drain connected loads, Current Source Loads, Noise and Distortion, Class AB Amplifier.

Feedback Equation, properties of negative feedback and amplifier design, feedback topologies, amplifiers employing the four types of feedback, Stability.

Unit III**DIFFERENTIAL AMPLIFIERS**

The Source Coupled pair, the Source Cross-Coupled pair, cascode loads, Wide-Swing Differential Amplifiers.

Unit IV

OPERATIONAL AMPLIFIERS

Basic CMOS Op-Amp Design, Operational Transconductance Amplifiers, Differential Output Op-Amp.

II. MIXED SIGNAL CIRCUITS:

Unit V

NON-LINEAR & DYNAMIC ANALOG CIRCUITS

Basic CMOS Comparator Design, Adaptive Biasing, Analog Multipliers, MOSFET Switch, Switched Capacitor circuits: Switched Capacitor Integrator, dynamic circuits.

Unit VI

DATA CONVERTER ARCHITECTURES

Data Converter Fundamentals, DAC & ADC specifications, Mixed Signal Layout issues, DAC architectures, ADC architectures.

TEXT BOOKS:

1. CMOS Circuit Design, Layout and Simulation - Baker, Li, Boyce, PHI, 2004.

REFERENCE BOOKS:

1. Analog Integrated Circuit Design - David A. Johns, Ken Martin, 1997, John Wiley & Sons
2. Design of Analog CMOS Circuits – B. Razavi, MGH, 2003, TMH.
3. Analog MOS ICs for Signal Processing – R.Gregorian, Gabor C. Temes, John Wiley & Sons.

I Year – II Sem. M.Tech.(DSCE)
DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES
(ELECTIVE III)

Code: 5U203

L T P C
3 1 - 3

a	b	c	d	e	f	g	h	i	j	k
X	X	X	X	X	X					

After completing the course students are able to understand

1. Analyse DSP tools such as DFT, FFT and systems such as LTI, LTV using MATLAB.
2. Obtain and understand the dynamic range, precision, conversional errors and computational errors
3. Learn basic architectural features and building blocks of Digital signal processor.
4. Understand and apply Execution control like hardware looping, interrupts and pipelining etc., analyze the processor TMS320C54XX processor.
5. Implement various DSP algorithms on TMS320C54XX.
6. Interface Memory and I/O peripherals to programmable DSP devices.

Unit I**INTRODUCTION TO DIGITAL SIGNAL PROCESING**

Introduction, A Digital signal-processing system, The sampling process, Discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation, Analysis and Design tool for DSP Systems MATLAB, DSP using MATLAB.

Unit II**COMPUTATIONAL ACCURACY IN DSP IMPLEMENTATIONS**

Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

Unit III**ARCHITECTURES FOR PROGRAMMABLE DSP DEVICES**

Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External interfacing.

Unit IV**EXECUTION CONTROL AND PIPELINING**

Hardware looping, Interrupts, Stacks, Relative Branch support, Pipelining and Performance, Pipeline Depth, Interlocking, Branching effects, Interrupt effects, Pipeline Programming models.

PROGRAMMABLE DIGITAL SIGNAL PROCESSORS

Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and

Programming, On-Chip Peripherals, Interrupts of TMS320C54XX processors, Pipeline Operation of TMS320C54XX Processors.

Unit V

IMPLEMENTATIONS OF BASIC DSP ALGORITHMS

The Q-notation, FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, PID Controller, Adaptive Filters, 2-D Signal Processing.

IMPLEMENTATION OF FFT ALGORITHMS

An FFT Algorithm for DFT Computation, A Butterfly Computation, Overflow and scaling, Bit-Reversed index generation, An 8-Point FFT implementation on the TMS320C54XX, Computation of the signal spectrum.

Unit VI

INTERFACING MEMORY AND I/O PERIPHERALS TO PROGRAMMABLE DSP DEVICES

Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).

A Multichannel buffered serial port (McBSP), McBSP Programming, a CODEC interface circuit, CODEC programming, A CODEC-DSP interface example.

TEXT BOOKS

1. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.
2. DSP Processor Fundamentals, Architectures & Features – Lapsley et al. S. Chand & Co, 2000.

REFERENCES

1. Digital Signal Processors, Architecture, Programming and Applications – B. Venkata Ramani and M.Bhaskar, TMH, 2002.
2. Digital Signal Processing – Jonatham Stein, John Wiley, 2005.

**I Year – II Sem. M.Tech.(DSCE)
RADAR SIGNAL PROCESSING
(ELECTIVE III)**

Code: 5U204

L T P C
3 1 - 3

a	b	c	d	e	f	g	h	i	j	k
X	X	X	X	X				X		

By the end of this course, students will be able to

1. *Understand elements of the radar range equation and Characterize radar signals in the time domain.*
2. *Learn basic concepts of the matched filter, correlation receiver.*
3. *Learn about detection of radar signals in presence of noise and also radar signal management.*
4. *Understand Radar Ambiguity Function , Family of Radar Waveforms and also Optimum Waveforms for Detection in Clutter.*
5. *Understand the Pulse Compression in Radar Signals.*
6. *Learn the concepts of phase coding Techniques*

Unit I

Introduction [1] – Radar Block Diagram, Radar Equation, Information Available from Radar Echo. Review of Radar Range Performance [2] – General Radar Range Equation, Radar Detection with Noise Jamming, Beacon and Repeater Equations, Bistatic Radar.

Unit II

Detection of Radar Signals in Noise - I [3] : Matched Filter Receiver – Impulse Response, Frequency Response Characteristic and its Derivation, Matched Filter and Correlation Function, Correlation Detection and Cross-Correlation Receiver. Efficiency of Non-Matched Filters, Matched Filter for Non-White Noise.

Unit III

Detection of Radar Signals in Noise - II [3] : Detection Criteria – Neyman-Pearson Observer, Likelihood-Ratio Receiver, Inverse Probability Receiver, Sequential Observer. Detectors – Envelope Detector, Logarithmic Detector, I/Q Detector. Automatic Detection - CFAR Receiver, Cell Averaging CFAR Receiver, CFAR Loss, CFAR Uses in Radar. Radar Signal Management – Schematics, Component Parts, Resources and Constraints.

Unit IV

Waveform Selection [3, 2] : Radar Ambiguity Function and Ambiguity Diagram – Principles and Properties; Specific Cases – Ideal Case, Single Pulse of Sine Wave, Periodic Pulse Train, Single Linear FM Pulse, Noise like Waveforms. Waveform Design Requirements. Optimum Waveforms for Detection in Clutter, Family of Radar Waveforms.

Unit V

Pulse Compression in Radar Signals : Introduction, Significance, Types. Linear FM Pulse Compression – Block Diagram, Characteristics, Reduction of Time Sidelobes, Stretch Techniques, Generation and Decoding of FM Waveforms – Block Schematic and Characteristics of Passive System, Digital Compression, SAW Pulse Compression.

Unit VI

Phase Coding Techniques: Principles, Binary Phase Coding, Barker Codes, Maximal Length Sequences (MLS/LRS/PN), Block Diagram of a Phase Coded CW Radar.

Text Books:

- 1) M.I. Skolnik, Radar Handbook, McGraw Hill, 2nd ed., 1991.
- 2) Fred E. Nathanson, Radar Design Principles – Signal Processing and The Environment, PHI, 2nd ed., 1999.
- 3) M.I. Skolnik, Introduction to Radar Systems, TMH, 3rd ed., 2001.

REFERENCES

- 1) Peyton Z. Peebles, Jr., Radar Principles, John Wiley, 2004.
- 2) R. Nit berg, Radar Signal Processing and Adaptive Systems, Artech House, 1999.
- 3) F.E. Nathanson, Radar Design Principles, McGraw Hill, 1st ed., 1969.
& Nelson Morgan, 1/e, Wiley

**I Year – II Sem. M.Tech.(DSCE)
Ad Hoc and Wireless Sensor Networks
(ELECTIVE III)**

Code: 5U205

L T P C
3 1 - 3

a	b	c	d	e	f	g	h	i	j	k
X	X	X	X	X	X					

By the end of this course, students will be able to

1. *Understand basics of Ad hoc Wireless Networks, MAC protocols for Ad hoc Wireless Networks.*
2. *Understand Routing protocols for Ad hoc Wireless Networks.*
3. *Understand Wireless sensor Networks.*
4. *Understand different routing techniques.*
5. *Understand the basics and issues of Wireless Sensor Networks.*
6. *Understand the difference and details of Random vs. structured Wireless Sensor Networks.*

Unit I**Ad Hoc Networks:**

Characteristics and Applications of Ad hoc Networks, Routing – Need for routing and routing, classifications, Table Driven Routing Protocols, Source Initiated On-Demand

Unit II

Routing Protocols, Hybrid, Protocols – Zone Routing, Fisheye Routing, LANMAR for MANET with group mobility, Location Added Routing, Distance Routing Effects, Microdiscovery and Power Aware Routing.

Unit III**Wireless Sensor Networks:**

Wireless Sensor Networks, DARPA Efforts, Classification, Fundamentals of MAC, Flat routing.

Unit IV**Routing:**

Directed Diffusion, SPIN, COGUR, Hierarchical Routing, Cluster base routing,

Unit V

Scalable Coordination, LEACH, TEEN, APTEEN and Adapting to the dynamic nature of Wireless Sensor Networks.

Unit VI

Random vs structured WSN:

Localization, Hierarchy , organization, Stationary vs. mobile, Energy efficient routing, sleeping modes, issues in WSNs.

Books Recommended

1. D.P. Agrawal and Qing-An zeng, “Introduction to Wireless and Mobile Systems” Thomson Learning
2. Martyn Mallick, Mobile and Wireless Design Essentials, Wiley, 2003
3. Kavesh Pahlavan and Prashant Krishnamurty - “Principles of Wireless Networks – A Unified Approach, Pearson Education, 2002

I Year – II Sem. M.Tech.(DSCE)
RF SYSTEM DESIGN
(ELECTIVE III)

Code: 5U206

L T P C
3 1 - 3

a	b	c	d	e	f	g	h	i	j	k
X	X	X	X	X	X					

By the end of this course, students will be able to

1. Understand about specifications and architectures of transceivers.
2. Familiar with homodyne and heterodyne receivers and some transmitters.
3. Accumulate with impedance matching and amplifiers knowledge.
4. Earn grip on feed back systems and power amplifiers.
5. Probe effectively with Phased locked loop and synthesizers.
6. Sufficiently confident on mixers and oscillators.

Unit I**CMOS PHYSICS, TRANSCIEVER SPECIFICATIONS AND ARCHITECTURES**

Introduction to MOSFET Physics, Noise: Thermal, shot, flicker, popcorn noise, Two port Noise theory, Noise Figure, THD, IP2, IP3, Sensitivity, SFDR, Phase noise - Specification distribution over a communication link,

Unit II

Homodyne Receiver, Heterodyne Receiver, Image reject, Low IF Receiver Architectures
 Direct upconversion Transmitter, Two step upconversion Transmitter

Unit III**IMPEDANCE MATCHING AND AMPLIFIERS**

S-parameters with Smith chart, Passive IC components, Impedance matching networks, Common Gate, Common Source Amplifiers, OC Time constants in bandwidth estimation and enhancement, High frequency amplifier design, Power match and Noise match, Single ended and Differential LNAs, Terminated with Resistors and Source Degeneration LNAs.

Unit IV**FEEDBACK SYSTEMS AND POWER AMPLIFIERS**

Stability of feedback systems: Gain and phase margin, Root-locus techniques, Time and Frequency domain considerations , Compensation, General model – Class A, AB, B, C, D, E and F amplifiers, Power amplifier Linearisation Techniques, Efficiency boosting techniques, ACPR metric, Design considerations

Unit V**PLL AND FREQUENCY SYNTHESIZERS**

Linearised Model, Noise properties, Phase detectors, Loop filters and Charge pumps, Integer-N frequency synthesizers, Direct Digital Frequency synthesizers

Unit VI

MIXERS AND OSCILLATORS

Mixer characteristics, Non-linear based mixers, Quadratic mixers, Multiplier based mixers, Single balanced and double balanced mixers, subsampling mixers, Oscillators describing Functions, Colpitts oscillators, Resonators, Tuned Oscillators, Negative resistance oscillators, Phase noise.

REFERENCES:

1. T.Lee, “Design of CMOS RF Integrated Circuits”, Cambridge, 2004.
2. B.Razavi, “RF Microelectronics”, Pearson Education, 1997.
3. Jan Crols, Michiel Steyaert, “CMOS Wireless Transceiver Design”, Kluwer Academic Publishers, 1997.
4. B.Razavi, “Design of Analog CMOS Integrated Circuits”, McGraw Hill, 2001.

**I Year – II Sem. M.Tech (DSCE)
EMBEDDED SYSTEMS LAB**

Code: 5U271

L T P C
- - 4 2

a	b	c	d	e	f	g	h	i	j	k
X	X	X	X	X	X			X		X

After going through the Laboratory course, the student will be able to

1. Write the basic assembly language and Embedded C programs for timer, serial communication etc.
2. Interface various devices such as keyboard, ADC, DAC, LCD, Stepper Motor with 8051 microcontroller.
3. Study the Real Time Operating Systems and its applications.
4. Develop the device drivers for RT Linux.
5. Develop the Serial Communication drivers for ARM processor.
6. Design of RTOS kernel and study of Compile/Assembler.

LIST OF EXPERIMENTS:

CYCLE 1 : 8051 MICROCONTROLLERS

Serial data Transmission using 8051 microcontroller in different modes

Look up tables for 8051

Timing subroutines for 8051 – Real time and applications

Keyboard interface to 8051

ADC, DAC interface to 8051

LCD interface to 8051

CYCLE 2 :

Study of Real Time Operating Systems

Development of Device Drivers for RT Linux

Software Development for DSP Applications

Serial Communication Drivers for ARM Processors

Case Studies : Any Two –

Design of RTOS Kernel

Cross Compiler / Assembler

Vx Works

**I Year -II Sem M.Tech. (VLSI & Embedded Systems)
LITERATURE REVIEW SEMINAR - 2**

Code: 5U272

L T P C
- - 3 1
Max. Marks: 100

a	b	c	d	e	f	g	h	i	j	k
X	X		X				X	X		

After studying this course, the students will be able to

1. Identify a research topic
2. Collect literature
3. Write technical review paper
4. Present seminar
5. Discuss the queries and Publish research paper

There shall be three seminar presentations during I year I semester and I year II Semester. For seminar, a student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the Department in a report form and shall make an oral presentation before the Departmental Committee, which shall consist of the Head of the Department, a senior Faculty Member and the Supervisor and will jointly evaluate the report and presentation. For each Seminar there will be only internal evaluation of 25 marks. A candidate has to secure a minimum of 50% to be declared successful.

In the First semester the report must be in the form of the review paper with a format used by IEEE / ASME etc. In the Second semester Technical Seminar in the form of Independent Review Paper must be of high quality fit for publication in a reputed conference / journal.

The evaluation format for seminar is as follows:

- Day to day evaluation by the Supervisor : 5 marks
- Final Report : 5 marks
- Presentation : 15 marks

A Student has to concentrate on the following sections while writing technical paper or presenting seminar.

Contents:

- Identification of specific topic
- Analysis
- Organization of modules
- Naming Conventions
- Writing style
- Figures
- Feedback
- Writing style
- Rejection
- Miscellaneous

REFERENCES:

Teach Technical Writing in Two Hours per Week by Norman Ramsey

For Technical Seminar the student must learn few tips from sample seminars and correcting himself, which is continues learning process

REFERENCE LINKS:

1. <http://www.cs.dartmouth.edu/~scot/givingTalks/sld001.htm>
2. <http://www.cse.psu.edu/~yuanxie/advice.htm>
3. <http://www.eng.unt.edu/ian/guides/postscript/speaker.pdf>

NOTE: A student can use any references for this process, but must be shared in classroom.

I Year – II Sem. M.Tech.(VLSI & Embedded Systems)
PROJECT SEMINAR – 1(Absract)

Code: 5U273

L	T	P	C
-	-	-	2

Max. Marks: 100

a	b	c	d	e	f	g	h	i	j	k
X	X	X	X				X	X		X

In I year II semester, a project seminar shall be conducted for 25 marks and for 2 credits (there is no external evaluation). The evaluation for the project seminar shall be done in two stages, i.e. in the middle of the semester and at the end of the semester. The mid-semester seminar evaluation shall carry 10 marks and the end semester seminar evaluation shall carry 15 marks. The report for the mid-semester project seminar will carry 5 marks and remaining marks shall be for presentation and discussion. The report for end semester project seminar shall be for 5 marks and the remaining marks shall be for presentation and discussion. A candidate shall secure a minimum of 50% to be declared successful.

**I Year –II Sem. M.Tech.(VLSI & Embedded Systems)
COMPREHENSIVE VIVA-VOCE - 2**

Code: 5U274

L	T	P	C
-	-	-	1

Max. Marks: 100

a	b	c	d	e	f	g	h	i	j	k
X	X						X	X		X

There shall be a Comprehensive Viva-Voce in II year I Semester. The Comprehensive Viva-Voce will be conducted by a Committee consisting of Head of the Department and two Senior Faculty members of the Department. The Comprehensive Viva-Voce is aimed to assess the students' understanding in various subjects he/she studied during the M.Tech course of study. The Comprehensive Viva-Voce is valued for 50 marks by the Committee. There are no internal marks for the Comprehensive Viva-Voce. A candidate has to secure a minimum of 50% to be declared successful.

II Year – I Sem. M.Tech.(VLSI & Embedded Systems)**PROJECT SEMINAR - 2****Code: 5U371**

L	T	P	C
-	-	-	2

Max. Marks100

a	b	c	d	e	f	g	h	i	j	k
X	X	X	X				X	X		X

In II year I semester, a project seminar shall be conducted for 50 marks and for 2 credits (there is no external evaluation). The evaluation for the project seminar shall be done in two stages, i.e. in the middle of the semester and at the end of the semester. The mid-semester seminar evaluation shall carry 20 marks and the end semester seminar evaluation shall carry 30 marks. The report for the mid-semester project seminar will carry 5 marks and remaining marks shall be for presentation and discussion. The report for end semester project seminar shall be for 10 marks and the remaining marks shall be for presentation and discussion. A candidate shall secure a minimum of 50% to be declared successful.

**II Year – I Sem. M.Tech (DSCE)
PROJECT WORK (PART I)
PROJECT STATUS REPORT**

Code: 5U373

L T P C
- - - 20

a	b	c	D	e	f	g	h	i	j	k
X	X	X	X	X	X	X	X	X	X	X

Every candidate shall be required to submit thesis or dissertation after taking up a topic approved by the Project Review Committee.

A Project Review Committee (PRC) shall be constituted comprising of Heads of all the Departments which are offering the M.Tech programs and three other senior faculty members concerned with the M.Tech. programme.

Registration of Project Work: A candidate is permitted to register for the project work after satisfying the attendance requirement of all the previous semesters and after obtaining the approval of the PRC.

After satisfying 6.2, a candidate has to submit, in consultation with his project supervisor, the title, objective and plan of action of his project work to the PRC for its approval. Only after obtaining the approval of PRC the student can initiate the Project work. This process is to be completed within four weeks of commencement of II year I semester.

The student shall submit a project report at the end of II year I semester, and the same shall be evaluated at the end of that semester by the PRC as Excellent/Good/Satisfactory/Unsatisfactory. In the case of Unsatisfactory declaration, the student shall re-submit the Project report after carrying out the necessary modifications / additions in the Project work, within the specified time as suggested by the PRC.

**II Year – II Sem. M.Tech (DSCE)
PROJECT SEMINAR-3**

Code: 5U471

L	T	P	C
-	-	-	2

Max. Marks: 100

a	b	c	d	e	f	g	h	i	j	k
X	X	X	X				X	X		X

A project seminar shall be conducted for 50 marks and for 2 credits (there is no external evaluation). The evaluation for the project seminar shall be done in two stages, i.e. in the middle of the semester and at the end of the semester. The mid-semester seminar evaluation shall carry 20 marks and the end semester seminar evaluation shall carry 30 marks. The report for the mid-semester project seminar will carry 5 marks and remaining marks shall be for presentation and discussion. The report for end semester project seminar shall be for 20 marks and the remaining marks shall be for presentation and discussion. A candidate shall secure a minimum of 50% to be declared successful.

II Year – II Sem. M.Tech (DSCE)
Pre submission Seminar SEMINAR-3

Code: 5U472

L	T	P	C
-	-	-	2

Max. Marks: 100

a	b	c	d	e	f	g	h	i	j	k
X	X	X	X				X	X		X

**II Year – II Sem. M.Tech (DSCE)
PROJECT WORK AND DISSERTATION**

Code: 5U473

L T P C
- - - 20

a	b	c	d	e	f	g	h	i	j	k
X	X	X	X	X	X	X	X	X	X	X

By the end of this course, students will be able to

1. Critically and theoretically analyze the systems/products they are going to design or develop.
2. Apply the theoretical knowledge gained to bring out innovative products.
3. Effectively communicate in a variety of forms including written, visual, verbal, online and technical literacy.
4. Work and participate as effective members in a group within a professional environment.
5. Develop an ongoing critical awareness of learning needs in the application of appropriate technologies.
6. Gain as much knowledge and experience in areas of the area of Digital Systems and Computer Electronics

A candidate is permitted to submit Project Dissertation only after successful completion of PG subjects (theory and practical), seminars, Comprehensive viva-voce, PG Project Part–I, and after the approval of PRC, not earlier than 40 weeks from the date of registration of the project work. For the approval of PRC the candidate shall submit the draft copy of thesis to the Head of the Department and shall make an oral presentation before the PRC. Along with the draft thesis the candidate shall submit draft copy of a paper in standard format fit for publication in Journal / Conference, based on the project thesis, to the Head of the Department with due recommendation of the supervisor.

- Four copies of the Project Dissertation certified by the Supervisor and Head of the Department shall be submitted to the College.
- The dissertation shall be adjudicated by one examiner selected by the College. For this, Head of Department shall submit a panel of 3 examiners, who are eminent in that field, with the help of the PRC. The Chief Superintendent of the college in consultation with the college academic committee shall nominate the examiner.
- If the report of the examiner is not favorable, the candidate shall revise and resubmit the Dissertation, in the time frame as prescribed by PRC. If the report of the examiner is unfavorable again, the thesis shall be summarily rejected. The candidate can re-register only once for conduct of project and evaluation of Dissertation, and will go through the entire process as mentioned above. The total duration for the M.Tech program is limited to four years.
- If the report of the examiner is favorable, viva-voce examination shall be conducted by a Board consisting of the Head of the Department, Supervisor and the Examiner who

adjudicated the Dissertation. The Board shall jointly report the student's performance in the project work as – (a) Excellent, or (b) Good, or (c) Satisfactory, or (d) Unsatisfactory, as the case may be. In case, the student fails in the viva-voce examination, or gets the Unsatisfactory grade, he can re-appear only once for the viva-voce examination, as per the recommendations of the Board. If he fails at the second viva-voce examination, the candidate can re-register only once for conduct of project and evaluation of Dissertation, and will go through the entire process as mentioned above. The total duration for the M.Tech program is limited to four years.