COURSE STRUCTURE
AND
DETAILED SYLLABUS

for

M.Tech course

in

VLSI & EMBEDDED SYSTEMS

(ECE)

(Applicable for the batches admitted from 2012-2013)

SREENIDHI INSTITUTE OF SCIENCE AND TECHNOLOGY
(An Autonomous Institution approved by UGC and affiliated to JNTUH)
Yamnampet, Ghatkesar, R.R.District-501 301.

Department of Electronics and Communication Engineering

M.Tech.(VLSI & Embedded Systems)
Course Structure and Syllabus
Academic Regulations : 2012

I YEAR - I Semester

Sl. No.	Code	Subject	L	T	P	Credits	Internal marks	External marks
1.	122VE01	VLSI Technology and Design	4	-	-	3	40	60
2.	122VE02	CPLD & FPGA Architectures and Applications	4	-	-	3	40	60
3.	122DS01	Digital System Design	4	-	-	3	40	60
4.	122DS03	Advanced Microprocessors and Microcontrollers	4	-	-	3	40	60
5.	122VE03 122VE04 122VE05	Elective-I	4	-	-	3	40	60
6.	122DS04 122VE06 122VE07	Elective-II	4	-	-	3	40	60
7.	122VE71	Simulation Lab (Verilog)	-	-	6	3	40	60
8.	122VE72	Technical Paper Writing and Seminar	-	-	3	2	50	-
		Total	**24**	**-**	**9**	**23**	**330**	**420**

I YEAR - II Semester

Sl. No.	Code	Subject	L	T	P	Credits	Internal marks	External marks
1.	122VE08	System on Chip Architecture	4	-	-	3	40	60
2.	122DS06	Design of Fault Tolerant Systems	4	-	-	3	40	60
3.	122VE09	Embedded Real Time Operating Systems	4	-	-	3	40	60
4.	122DS07	CMOS Analog & Mixed Signal Design	4	-	-	3	40	60
5.	122MB01 122SE20 122SE21 122SE22	Open Elective	4	-	-	3	40	60
6.	122DS05 122DS08 122VE10	Elective-III	4	-	-	3	40	60
7.	122VE73	Embedded Systems Lab	-	-	6	3	40	60
8.	122VE74	Technical Seminar (Independent Review Paper)	-	-	3	2	50	-
		Total	**24**	**-**	**9**	**23**	**330**	**420**

M.Tech. (VLSI & Embedded Systems)
Course Structure and Syllabus:Year
Academic Regulations : 2012

II YEAR – I Semester

Sl. No.	Code	Subject	L	T	P	Credits	Internal marks	External marks
1.	122VE75	Comprehensive Viva-Voce	-	-	-	2	-	50
2.	122VE76	Project Seminar	-	-	-	2	50	-
3.	122VE77	Project Work (Part I)	-	-	-	18	Grading*	-
		Total	-	-	-	**22**	**50**	**50**

*****Grading – Excellent/ Good/ Satisfactory/ Unsatisfactory

II YEAR – II Semester

Sl. No.	Code	Subject	L	T	P	Credits	Internal marks	External marks
1.	122VE78	Project Seminar	-	-	-	2	50	-
2.	122VE79	Project Work and Dissertation	-	-	-	20	-	Grading*
		Total	-	-	-	**22**	**50**	**-**

*Grading – Excellent / Good/ Satisfactory/ Unsatisfactory

ELECTIVE I

1) 122VE03 - Hardware Software Co-Design
2) 122VE04 - Device Modeling
3) 122VE05 - Algorithms for VLSI Design Automation

ELECTIVE II

1) 122DS04 - Advanced Digital Signal Processing
2) 122VE06 - Low Power VLSI Design
3) 122VE07 - Nanoelectronics

OPEN ELECTIVE

1) 122MB47 - Entrpreneurship and Innovation
2) 122SE20 - Network Security & Cryptography
3) 122SE21 - Advanced Operating Systems
4) 122SE22 - Research Methodology

ELECTIVE III

1) 122DS05 - Image & Video Processing
2) 122DS08 - Digital Signal Processors and Architectures
3) 122VE10 - Semiconductor Memory Design & Testing

I Year – I Sem. M.Tech. (VLSI&ESs)
VLSI TECHNOLOGY & DESIGN

Code : 122VE01

L	T	P	C
4	-	-	3

UNIT – I:

Review of Microelectronics and Introduction to MOS Technologies: MOS, CMOS, BiCMOS Technology, Trends And Projections.

Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits: I_{ds}-V_{ds} relationships, Threshold Voltage V_t, g_m, g_{ds} and ω_o, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT – II:

LAYOUT DESIGN AND RULES: Stick diagrams, MOS Layers, Layout diagrams,Design rules for wires (nMOS and CMOS), Transistor Design rules, Design rules for Contacts in NMOS ckts, Buried and butting contacts.

UNIT – III:

LOGIC GATES: Static Complementary Gates, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT – IV:

COMBINATIONAL LOGIC NETWORKS: Standard Cell Based Layout Design, Simulation, Combinational Network delay, Interconnect design, Power optimization, Switch logic networks, Gate and Network testing.

UNIT –V:

SEQUENTIAL SYSTEMS: Latches and Flip-Flops,, Clocking disciplines, Design, Power optimization, Design validation and testing.

UNIT – VI:

FLOOR PLANNING: Floor planning methods, off-chip connections.

ARCHITECTURE DESIGN: High-level synthesis, Architecture for low power, SOCs and Embedded CPUs, Architecture testing.

TEXT BOOKS:

1. Essentials of VLSI Circuits and Systems, K. Eshraghian, Douglas A.Pucknell, 2005, PHI.

2. Modern VLSI Design - Wayne Wolf, 3rd ed., 1997, Pearson Education.

REFERENCES:

1. Principals of CMOS VLSI Design – N.H.E Weste, K.Eshraghian, 2nd ed., Adisson Wesley.

2. Digital Integrated Circuits A Design Perspective – Jan M.Rabaey, Ananta Chandrakasan, Borivoje Nikolic, Pearson Education

3. Principles of CMOS VLSI Design A System Perspective – Neil H.E.Weste, K. Eshraghian, Addison-Wesley Publishing Company.

4. Introduction to VLSI Circuits and Systems – John Uyemura, John Willey & Sons, Inc

5. VLSI design techniques for Analog and Digital Circuits – Randall L.Geiger, Phillip E.Allen, Noel R.StraderMcGraw-Hill Company

6. CMOS/BiCMOS ULSI Low Voltage, Low Power – Kiat-Seng Yeo, Samir S.Rofail, Wang-Ling Goh

I Year – I Sem. M.Tech. (VLSI & Embedded Systems)
CPLD & FPGA ARCHITECTURE AND APPLICATIONS

Code: 122VE02

L	T	P	C
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UNIT –I

Programmable logic : ROM, PLA, PAL PLD, PGA – Features, programming and applications using complex programmable logic devices Altera series – Max 5000/7000 series and Altera FLEX logic-10000 series CPLD - Speed performance and in system programmability.

UNIT –II

Programming and applications using AMD's- CPLD (Mach 1to 5), Cypres FLASH 370 Device technology, Lattice PLST's architectures – 3000 series – Speed performance and in system programmability.

UNIT – III

FPGAs: Field Programmable gate arrays- Logic blocks, routing architecture, design flow technology mapping jfor FPGAs, Case studies Xitir x XC4000 & ALTERA's FLEX 8000/10000 FPGAs: AT &T ORCA's (Optimized Reconfigurable Cell Array): ACTEL's ACT-1,2,3 and their speed performance

UNIT-IV

Alternative realization for state machine chat using microprogramming linked state machine one –hot state machine, Petri Nets for state machines-basic concepts, properties, and extended Petri Nets for parallel controllers. , Encode State Machines- Traffic Light Controller-Implementation of Petri-net description.

UNIT-V

Digital front end digital design tools for FPGAs & ASICs: Using EDA tools – Design flow using FPGAs. Software Tool box - Placement, Routing & wire ability.

UNIT - VI

Case studies of parallel adder cell, parallel adder sequential circuits, counters, multiplexers, parellel controllers.

TEXT BOOKS:

1. Field Programmable Gate Array Technology - S. Trimberger, Edr, 1994, Kluwer Academic Publications.

2. Field Programmable Gate Arrays, John V.Oldfield, Richard C Dore, Wiley Publications.

3. Field programmable gate array, S. Brown, R.J.Francis, J.Rose ,Z.G.Vranesic, 2007, BSP.

REFERENCES:

1. Digital Design Using Field Programmable Gate Array, P.K.Chan & S. Mourad, 1994, Prentice Hall.
2. Digital System Design using Programmable Logic Devices – Parag.K.Lala, 2003, BSP.
3. Data Sheets of XILINX & ALTERA
4. Digital Systems Design with FPGA's and CPLDs – Ian Grout, 2009, Elsevier.

I Year – I Sem. M.Tech.(VLSI & Embedded Systems)
DIGITAL SYSTEM DESIGN

Code : 122DS01

L	T	P	C
4	-	-	3

Unit-I: Designing with Programmable Logic Devices

Designing with Read only memories – Programmable Logic Arrays – Programmable Array logic – Sequential Programmable Logic Devices – Design with FPGA's– Using a One-hot state assignment,

State transition table- State assignment for FPGA's - Problem of Initial state assignment for One –Hot encoding - State Machine charts – Derivation of SM Charts – Realization of SM charts – Design Examples –Serial adder with Accumulator - Binary Multiplier – Dice Game controller – Binary Divider – Control logic for Sequence detector – Realization with Multiplexer – PLA – PAL.

Unit-II: Fault Modeling

Logic Fault model – Fault detection & Redundancy- Fault equivalence and fault location –Fault dominance – Single stuck at fault model – Multiple stuck at fault models –Bridging fault model

Fault diagnosis of combinational circuits by conventional methods – Path sensitization techniques, Boolean Difference method – Kohavi algorithm, Test Algorithms- D-Algorithm.

Unit-III: Test Pattern Generation

Random testing, Transition count testing, Exhaustive Testing and Pseudo Random Testing. Signature analysis and test bridging faults.

Unit-IV: Fault Diagnosis in Sequential Circuits

Circuit Test Approach, Transition Check Approach - State identification and fault detection experiment, Machine identification, Design of fault detection experiment.

Unit-V: PLA Minimization and Testing

PLA Minimization – PLA folding, Fault model in PLA, Test generation and Testable PLA Design.

Unit-VI: Minimization and Transformation of Sequential Machines

The Finite state Model – Capabilities and limitations of FSM – State equivalence and machine minimization – Simplification of incompletely specified machines.

Fundamental mode model – Flow table – State reduction – Minimal closed covers – Races, Cycles and Hazards.

TEXT BOOKS:

1. Fundamentals of Logic Design – Charles H. Roth, 5th ed., Cengage Learning.
2. Digital Systems Testing and Testable Design – Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman- John Wiley & Sons Inc.
3. Switching and Finite Automata Theory – Z. Kohavi , 2nd ed., 2001, TMH
4. Logic Design Theory – N. N. Biswas, PHI

REFERENCES :

1. Digital Design – Morris Mano, M.D.Ciletti, 4th Edition, PHI.
2. Digital Circuits and Logic Design – Samuel C. Lee , PHI

I Year – I Sem. M.Tech.(DSCE)
ADVANCED MICROPROCESSORS AND MICROCONTROLLERS

Code: 122DS03

L	T	P	C
4	-	-	3

UNIT-I
8086 microprocessor family overview, 8086 Internal Architecture, memory interfacing constructing the machine codes for 8086, Introduction to programming the 8086, writing programes with Assembler, Assembly Language program development tools.

UNIT-II
The 80286, 80386, 80486 and Pentium processors – The Intel 80286 microprocessor, The Intel 80386 32-Bit microprocessor architecture, The Intel 80486 microprocessor and pentium processor architecture concept of multiuser / multitasking operating system.

UNIT-III
Interfacing to 8086 microprocessor, 8086 Interrupts and Interrupt applications, Digital Interfacing, Analog interfacing and Industrial Control, DMA, Cache Memory and co-processors.

UNIT-IV
Introduction to ARM processor -Programming model – ARM Development Tools – ARM instruction set execution and implementation – ARM coprocessor interface.
ARM Processor as System-on-Chip: Acorn RISC machine – Architecture inheritance –3 and 5 stage pipeline ARM organization.

UNIT-V
ARM assembly language programming: ARM instruction types – data transfer, data processing and control flow instructions – ARM instruction set – Coprocessor instructions.
Architectural support for high level language: Data types – abstraction in software design – Expressions – Loops – Functions and Procedures – Conditional statements – use of memory.

UNIT-VI
Simple applications of microprocessors and microcontrollers using ARM 9 processors, Robot control, stepper motor control, interfacing of analog and digital sensors, process control, measuring of parameters like – pressure, temperature, level, position, etc., using microcontrollers. Standard interfaces like Centronics, IEEE-488, USB and RS-232.

TEXT BOOKS:

1. Microprocessors and Interfacing by DOUGLAS V HALL, Revised Second Edition.
2. Computers and Components, Wayne Wolf, Elseveir.

REFERENCES:

1. ARM Technical references
2. Embedded System Design, Frank Vahid, Tony Givargis, John Wiley.
3. Microcontrollers, Raj Kamal, Pearson Education.
4. An Embedded Software Primer, David E. Simon, Pearson Education.

I Year – I Sem. M.Tech.(VLSI & Embedded Systems)
HARDWARE- SOFTWARE CO-DESIGN
(ELECTIVE-I)

Code: 122VE03

L	T	P	C
4	-	-	3

UNIT –I

CO- DESIGN ISSUES

Co- Design Models, Architectures, Languages, a Generic Co-design Methodology.

CO- SYNTHESIS ALGORITHMS

Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT –II

PROTOTYPING AND EMULATION

Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

UNIT -III

TARGET ARCHITECTURES

Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT – IV

COMPILATION TECHNIQUES AND TOOLS FOR EMBEDDED PROCESSOR ARCHITECTURES

Modern embedded architectures, embedded software development needs, compilation technologies practical consideration in a compiler development environment.

UNIT – V

DESIGN SPECIFICATION AND VERIFICATION

Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

UNIT – VI

LANGUAGES FOR SYSTEM – LEVEL SPECIFICATION AND DESIGN-I

System – level specification, design representation for system level synthesis, system level specification languages

LANGUAGES FOR SYSTEM – LEVEL SPECIFICATION AND DESIGN-II

Heterogeneous specifications and multi language co-simulation the cosyma system and lycos system.

TEXT BOOKS

1. Hardware / software co- design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – 2009, Springer.
2. Hardware / software co- design Principles and Practice, 2002, Kluwer Academic Publishers

I Year – I Sem
DEVICE MODELING (ELECTIVE-I)

Code: 122VE04

L	T	P	C
4	-	-	3

UNIT I

Introduction to Semiconductor Physics: Review of Quantum Mechanics, Boltzman transport equation, continuity equation, Poisson equation

Integrated Passive Devices: Types and Structures of resistors and capacitors in monolithic technology, dependence of model parameters on structures

UNIT II

Integrated Diodes: Junction and Schottky diodes in monolithic technologies – static and dynamic behavior – small and large signal models – SPICE models

UNIT III

Integrated Bipolar Transistor: Types and structures in monolithic technologies – Basic model (Eber-Moll) – Gummel - Poon model- dynamic model, parasitic effects – SPICE model –parameter extraction

UNIT IV

Integrated MOS Transistor: nMOS and pMOS transistor – threshold voltage – threshold voltage equations – MOS device equations – Basic DC equations second order effects –Advanced MOSFET Modeling, challenges in Advanced modeling and the study of the universal MOSFET Model. MOS FET SPICE model level 1, 2, 3 and 4

UNIT V

VLSI Fabrication Techniques: An overview of wafer fabrication, wafer processing – oxidation – patterning – diffusion – ion implantation – deposition – Silicon gate nMOS process – CMOS processes – n-well- p-well- twin tub- Silicon on insulator – CMOS process enhancements – interconnects circuit elements

UNIT VI

Modeling of Hetero Junction Devices: Band gap Engineering, Bandgap Offset at abrupt Hetero Junction, Modified current continuity equations, Hetero Junction bipolar transistors (HBTs), SiGe

TEXT BOOKS

1. Introduction to Device Modeling and Circuit Simulation –Tor. A. Fijedly- Wiley Interscience, 1997
2. Introduction to Semiconductor Materials and Devices – Tyagi M. S, 2008, John Wiley Student Edition.
3. Solid state circuits – Ben G. Streetman, Prentice Hall, 1997

REFERENCE BOOKS

1. Physics of Semiconductor Devices – Sze S. M, 2nd edition, Mcgraw hill, New York, 1981.

I Year – I Sem.
ALGORITHMS FOR VLSI DESIGN AUTOMATION
(ELECTIVE-I)

Code: 122VE05

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4	-	-	3

UNIT I
PRELIMINARIES
Introduction to Design Methodologies, Design Automation tools, Algorithmic Graph Theory, Computational complexity, Tractable and Intractable problems.

UNIT II
GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION
Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming,
Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

UNIT III
LAYOUT COMPACTION, PLACEMENT, FLOORPLANNING AND ROUTING
Problems, Concepts and Algorithms.
MODELLING AND SIMULATION
Gate Level Modelling and Simulation, Switch level Modelling and Simulation.

UNIT IV
LOGIC SYNTHESIS AND VERIFICATION
Basic issues and Terminology, Binary-Decision diagrams, Two-Level logic Synthesis
HIGH-LEVEL SYNTHESIS
Hardware Models, Internal representation of the input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aspects of Assignment problem, High-level Transformations.

UNIT V
PHYSICAL DESIGN AUTOMATION OF FPGAs
FPGA technologies, Physical Design cycle for FPGAs, partitioning and Routing for segmented and staggered Models.

UNIT VI
PHYSICAL DESIGN AUTOMATION OF MCMs
MCM technologies, MCM physical design cycle, Partitioning, Placement - Chip Array based and Full Custom Approaches, Routing – Maze routing, Multiple stage routing, Topologic routing, Integrated Pin – Distribution and routing, Routing and Programmable MCMs.

TEXT BOOKS

1. Algorithms for VLSI Design Automation, S.H.Gerez, 1999, WILEY Student Edition, John wiley & Sons (Asia) Pvt. Ltd.
2. Algorithms for VLSI Physical Design Automation – Naveed Sherwani, 3rd Ed., 2005, Springer International Edition.

REFERENCE BOOKS

1. Computer Aided Logical Design with Emphasis on VLSI – Hill & Peterson, 1993, Wiley.
2. Modern VLSI Design:Systems on silicon – Wayne Wolf, 2nd ed., 1998, Pearson Education Asia.

I Year – I Sem.
ADVANCED DIGITAL SIGNAL PROCESSING (ELECTIVE-I)

Code : 122DS04

L	T	P	C
4	-	-	3

UNIT I

DISCRETE FOURIER TRANSFORMS: Frequency domain Sampling, Properties of DFT, Linear Filtering Methods based on the DFT,Frequency Analysis of Signals using DFT.

UNIT II

FAST FOURIER TRANSFORMS: Radix-2, Radix-4, Split Radix FFT Algorithms, The Goertzel Algorithm and Chrip-z Transform Algorithm.

UNIT III

DESIGN OF IIR FILTERS: Design of IIR Filters using Butterworth and Chebyshev Approximations, Structures for IIR Systems –Direct Form, Cascade, Parallel, Lattice and Lattice-Ladder Structures.

UNIT –IV

DESIGN OF FIR FILTERS: Fourier series method, Windowing Techniques, Design of Digital Filters based on Least-Squares Method, Structures for FIR Systems –Direct Form, Cascade, Lattice Structures.

UNIT V

MULTIRATE SIGNAL PROCESSING: Introduction, Decimation by a factor D, Interpolation by a factor I, Sampling rate conversion by a rational factor I/D, Filter design & Implementation for sampling rate conversion.

UNIT VI

Linear Prediction : Forward and Backward Linear Prediction – Forward Linear Prediction, Backward Linear Prediction, Optimum reflection coefficients for the Lattice Forward and Backward Predictors. Solution of the Normal Equations: Levinson Durbin Algorithm, Schur Algorithm. Properties of Linear Prediction Filters

TEXT BOOKS

1. Digital Signal Processing: Principles, Algorithms and Applications - J.G.Proakis & D.G.Manolokis, 4th ed., PHI.
2. Discrete Time signal processing - Alan V Oppenheim & Ronald W Schaffer, PHI.
3. DSP – A Practical Approach – Emmanuel C.Ifeacher, Barrie. W. Jervis, 2nd ed., Pearson Education.

REFERENCE BOOKS

1. Digital Spectral Analysis with applications– S. Lawrence Marple Jr, Prentice-Hall Series in Signal Processing.
2. Modern spectral Estimation : Theory & Application – S. M .Kay, 1988, PHI.
3. Multirate Systems and Filter Banks – P.P.Vaidyanathan – Pearson Education
4. Digital Signal Processing – S.Salivahanan, A.Vallavaraj, C.Gnanapriya, 2000,TMH

I Year – I Sem.
LOW POWER VLSI DESIGN
(ELECTIVE-II)

Code: 122VE06

L	T	P	C
4	-	-	3

UNIT I

INTRODUCTION: low power design - an over view, **L**ow-Voltage, Low power design limitations, Silicon-on-Insulator Technology.

MOS/BiCMOS PROCESSES-Technology and Integration: Introduction, The realization of BiCMOS processes, BiCMOS manufacturing and Integration considerations, Isolation in BiCMOS.

UNIT II

DEEP SUBMICRON PROCESSES: Polysilicon Emitter High-Performance BiCMOS Structure, Low capacitance Bipolar/BiCMOS Processes,SOI CMOS/BiCMOS VLSIs.

LOW-VOLTAGE/LOW POWER CMOS/ BICMOS PROCESSES: Low Voltage/Low Power SOI CMOS, Low Voltage/Low Power Lateral BJT on SOI, Future trends and Directions of CMOS/BiCMOS processes.

UNIT III

CMOS AND Bi-CMOS LOGIC GATES: Conventional CMOS and BiCMOS logic gates. Performance evaluation

UNIT IV

LOW- VOLTAGE LOW POWER LOGIC CIRCUITS-1: BiCMOS Circuits Utilizing Lateral pnp BJTs in pMOS Structures, Merged BiCMOS Digital Circuits, Full-Swing Multi Drain/Multi Collector Complementary BiCMOS Buffers, Qasi Complementary BiCMOS Digital Circuits, Full-Swing BiCMOS/BiNMOS Digital Circuits Employing Schottky Diodes.

UNIT V

LOW- VOLTAGE LOW POWER LOGIC CIRCUITS-2: Feedback type BiCMOS Digital Circuits, High-Beta BiCMOS Digital Circuits, Transiently Saturated Full-Swing BiCMOS Digital Circuits, Bootstrapped-Type BiCMOS Digital Circuits, ESD-free Bi CMOS Digital Circuit.

UNIT VI

LOW POWER LATCHES AND FLIP FLOPS: Evolution of Latches and Flip flops-quality measures for latches and Flip flops, Design perspective.

TEXT BOOKS

1. CMOS/BiCMOS ULSI low voltage, low power by Yeo Rofail/ Gohl(3 Authors)-Pearson Education Asia 1st Indian reprint,2002

REFERENCES

1. Digital Integrated circuits , J.Rabaey PH. N.J 1996

2. CMOS Digital ICs , Sung-moKang and Yusuf Leblebici 3rd edition TMH 2003 (chapter 11)

3. VLSI DSP systems , Parhi, John Wiley & sons, 2003 (chapter 17)

4. IEEE Trans Electron Devices, IEEE J.Solid State Circuits, and other National and International Conferences and Symposia

I Year – I Sem.
NANOELECTRONICS
(ELECTIVE-II)

Code: 122VE07

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UNIT I
INTRODUCTION TO PHYSICS OF SOLID STATE: Structure – Size dependence of properties, crystal structures, Face centered cubic nanoparticles, tetraherally bonded semiconductor structures, lattice vibrations, Energy bands – insulators, semiconductors and conductors, reciprocal space, energy bonds and gaps of semiconductors, effective masses, Fermi surfaces, Localized particles – donors, acceptors and deep traps, mobility, excitons.

UNIT II
BASICS OF NANOELECTRONICS: Electromagnetic Fields and Photons, Quantization of Action, Charge and Flux, Electrons behaving as waves, Electrons in potential wells, Photons interacting with electrons in solids, Diffusion Processes.

UNIT III
QUANTUM ELECTRONICS: Quantum electronic devices (QED): Upcoming electronic devices, Electrons in Mesoscopic structures, Examples of Quantum Electronic Devices: Short-Channel MOS Transistor, Split-Gate Transistor, Electron–Wave Transistor, Electron-Spin Transistor, Quantum Cellular Automata (QCA), Quantum Dot Array.

UNIT IV
MOLECULAR ELECTRONICS: Switches based on Fullerenes and Nanotubes, Polymer Electronics, Self-Assembling Circuits, Optical Molecular Memories.

UNIT V
NANOELECTRONICS WITH TUNNELLING DEVICES: Tunnelling Element (TE) – Tunnel effect and tunneling elements, Tunelling diode (TD), Resonant Tunnelling diode (RTD), Three-terminal resonant tunneling devices, Technology of RTD.

Digital Circuit design based on RTDs: Memory applications, basic logic circuits, Dynamic logic circuits, Digital circuit design based on RTBT (resonant tunneling bipolar transistor): RTBT mobile, RTBT threshold gate, RTBT multiplexer.

UNIT VI
a) SINGLE ELECTRON TRANSISTOR (SET): Principle of the Single-Electron Transistor: the Coulomb blockade, performance of the single electron transistor, technology, SET circuit design: wiring and drivers, logic and memory circuits, SET adder as an example of a distributed circuit, comparison between FET and SET circuit designs.

b) NANOMACHINES AND NANODEVICES: Microelectromechanical Systems (MEMS), Nanoelectromechanical Systems (NEMS) – Fabrication, Nanodevices and Nanomachines.

TEXT BOOKS:

1. Nanoelectronics and Nanosystems: From Transistors to Molecular and Quantum Devices, by Karl Goser, K. Glosekotter, J. Dienstuhl, Springer, third reprint 2009.

2. Introduction to Nanotechnology, by Charles Poole and Frank Owens, Wiley India, 2007.

REFERENCES:

1. Nanotechnology and Nano Electronics – Materials, devices and measurement Techniques by W.R. Fahrner; Springer.

2. Nano: The Essentials – Understanding Nano Scinece and Nanotechnology by T.Pradeep; Tata Mc.Graw Hill.

3. W. Ranier, “Nano Electronics and Information Technology”, Wiley, (2003).

4. K.E. Drexler, “Nano Systems”, Wiley, (1992).

5. Encylopedia of Nanotechnology by H.S. Nalwa, American Scientific Publishers

I Year – I Sem.
SIMULATION LAB (Verilog)

Code: 122VE71

L	T	P	C
-	-	4	2

Design of Experiments:
Statistical methods, Randomised block design, Latin and orthogonal squares, factorial design, Replication and randomization.

Data Analysis: Deterministic and random data, uncertainty analysis, tests for significance: Chi-square, student's 't' test, regression modeling, direct and interaction effects, ANOVA, F-test, Time series analysis, Autocorrelation and autoregressive modeling.

Text Book:
1. "The Design and Analysis of industrial Experiments", Davis. O. V.; Longman, London.

LIST OF EXPERIMENTS:

CYCLE 1:

1. Digital Circuits Description using Verilog.
2. Verification of the functionality of designed Circuits using function simulator.
3. Timing Simulation for critical Path time calculation.
4. Synthesis of Digital Circuits.
5. Place and route techniques for major FPGA Vendors using Xilinx, Altera, Cypress etc.,
6. Implementation of Designed Digital Circuits Using FPGA and CPLD devices.

CYCLE 2:

1. MoS inverter DC Characteristics, AC Characteristics, Transient Analysis.
2. NMOS, PMOS Characteristics.
3. Layout basics- INV, NAND, NOR, EXOR, EXNOR.
4. Layout of adder, subtractor, multiplexer.
5. Layout Comparator.

For Experiments in cycle 2: 3,4,5: Draw the Schematics Perform Simulation, Extract the Layout, Run Physical Verification (DRC, LVS, PEX) and post layout simulation.

I Year – I Sem. M.Tech.(VLSI & Embedded Systems)
TECHNICAL PAPER WRITING AND SEMINAR

Code: 122VE72

L	T	P	C
-	-	3	2

Max. Marks: 50

There shall be two seminar presentations during I year I semester and I year II Semester. For seminar, a student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the Department in a report form and shall make an oral presentation before the Departmental Committee, which shall consist of the Head of the Department, a senior Faculty Member and the Supervisor and will jointly evaluate the report and presentation. For each Seminar there will be only internal evaluation of 50 marks. A candidate has to secure a minimum of 50% to be declared successful.

In the First semester the report must be in the form of the review paper with a format used by IEEE / ASME etc. In the Second semester Technical Seminar in the form of Independent Review Paper must be of high quality fit for publication in a reputed conference / journal.

The evaluation format for seminar is as follows:

- Day to day evaluation by the Supervisor : 10 marks
- Final Report : 10 marks
- Presentation : 30 marks

A Student has to concentrate on the following sections while writing technical paper or presenting seminar.

Contents:

- Identification of specific topic
- Analysis
- Organization of modules
- Naming Conventions
- Writing style
- Figures
- Feedback
- Writing style
- Rejection
- Miscellaneous

REFERENCES:

Teach Technical Writing in Two Hours per Week by Norman Ramsey

For Technical Seminar the student must learn few tips from sample seminars and correcting himself, which is continues learning process

REFERENCE LINKS:

1. http://www.cs.dartmouth.edu/~scot/givingTalks/sld001.htm
2. http://www.cse.psu.edu/~yuanxie/advice.htm
3. http://www.eng.unt.edu/ian/guides/postscript/speaker.pdf

NOTE: A student can use any references for this process, but must be shared in classroom.

I Year – II Sem.
SYSTEM-ON-CHIP ARCHITECTURE

Code: 122VE08

L	T	P	C
4	-	-	3

UNIT I:
Introduction to processor design: Abstraction in hardware design, MUO a simple processor, Processor design trade off, design for low power consumption.

UNIT II:
ARM Processor as System-on-Chip: Acorn RISC machine – Architecture inheritance – ARM programming model – ARM development tools – 3 and 5 stage pipeline ARM organization – ARM instruction execution and implementation – ARM coprocessor interface.

UNIT III:
ARM assembly language programming: ARM instruction types – data transfer, data processing and control flow instructions – ARM instruction set – Coprocessor instructions.
Architectural support for high level language: Data types – abstraction in software design – Expressions – Loops – Functions and Procedures – Conditional statements – use of memory.

UNIT IV:
Memory Hierarchy: Memory size and speed – on chip memory – caches – cache design - an example – memory management.

UNIT V:
Architectural support for System Management: Advanced microcontroller bus architecture – ARM memory interface – ARM reference peripheral specification – Hardware system prototyping tools – Armulator – Debug architecture.

UNIT VI:
Architectural support for Operating System: An introduction to Operating Systems – ARM system control coprocessor – CP15 protection unit registers – ARM protection unit – CP15 MMU registers – ARM MMU architecture – Synchronization – Context switching input and output.

TEXT BOOKS
1. ARM System on Chip Architecture, Steve Furber, 2nd ed. 2000, Addison Wesley Professional.
2. Design of System on a Chip: Devices and Components, Ricardo Reis, 1st ed. 2004, Springer.

REFERENCE BOOKS
1. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology), Jason Andrews, Newnes, BK and CDROM.
2. System on Chip Verification: Methodologies and Techniques, Prakash Rasnikar, Peter Paterson and Leena Singh L, Kluwer Academic Publishers.

I Year – II Sem. M.Tech.(VLSI & Embedded Systems)
DESIGN OF FAULT TOLERANT SYSTEMS

Code: 122DS06

L	T	P	C
4	-	-	3

UNIT I

BASIC CONCEPTS: Reliability concepts, Failure & Faults, Reliability and failure rate, Relation between reliability and Meantime between failure, Maintainability and Availability, Reliability of series, Parallel and Parallel-Series combinational circuits.

FAULT TOLERANT DESIGN: Basic concepts – Static, dynamic, hybrid, Triple Modular Redundant System, Self purging redundancy, Siftout redundancy (SMR), 5 MR re-configuration techniques, Use of error correcting code, Time redundancy and software redundancy.

UNIT II

SELF CHECKING CIRCUITS: Basic concepts of Self checking circuits, Design of Totally Self Checking checker, Checkers using m out of n codes, Berger code, Low cost residue code.

FAIL SAFE DESIGN: Strongly fault secure circuits, fail safe design of sequential circuits using partition theory and Berger code, Totally self checking PLA design.

UNIT III

Introduction to ATPG, ATPG process – Testability and Fault Analysis methods, Fault masking, Transition delay fault ATPG, Path delay, fault ATPG.

UNIT IV

DESIGN FOR TESTABILITY FOR COMBINATIONAL CIRCUITS: Basic concepts of testability, controllability and observability, the Reed Muller's expansion technique, OR-AND-OR design, use of control and syndrome testable designs.

UNIT V

Scan Architectures and Techniques: Introduction to scan based testing, functional testing, the scan effective circuit, the MUX-D style scan flip-flops, the scan shift register, scan cell operation.

Scan Test Sequencing, scan test timing, partial scan, multiple scan chains, scan based design rules (LSSD), At-speed scan testing and architecture, multiple clock and scan domain operation, critical paths for At-speed scan test. Boundary Scan Test: JTAG Test Operations

UNIT VI

BUILT IN SELF TEST (BIST): BIST concepts, Test pattern generation for BIST exhaustive testing, Pseudorandom testing, pseudo exhaustive testing, constant weight patterns, Generic offline BIST architecture, memory test architecture.

TEXT BOOKS:

1. Fault Tolerant & Fault Testable Hardware Design - Parag K. Lala, PHI

2. Design for Test for Digital ICs and Embedded Core Systems – Alfred L. Crouch, 2008, Pearson Education.

3. Fundamentals of Logic Design – Charles H. Roth, 5th ed., Cengage Learning.

REFERENCES:

1. Digital Systems Testing and Testable Design - M. Abramovili, M.A. Breues, A. D. Friedman, Jaico publications.

2. Essentials of Electronic Testing – Bushnell, and Vishwani D. Agarwal, Springers.

I Year – II Sem. M.Tech.(VLSI & Embedded Systems)
EMBEDDED REAL TIME OPERATING SYSTEMS

Code: 122VE09

L	T	P	C
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Unit I: Introduction
Embedded systems overview, design challenges, processor technology, I.C. technology, design technology, trade-offs. Single purpose processors, optimizing custom single purpose processors and general purpose processors, ASIPS, microcontrollers and DSP processors for embedded systems.

Unit II: Real Time Systems:
Typical real time applications, Hard Vs Soft real-time systems, A reference model of Real Time Systems: Processors and Resources, Temporal Parameters of real Time Work load, Periodic task model precedence constraints and data dependency, functional parameters, Resource Parameters of jobs and parameters of resources.

Unit III: Scheduling
Commonly used Approaches to Real Time Scheduling Clock Driven, Weighted Round Robin, Priority Driven, Dynamic Vs State Systems, Effective release time and Dead lines, Offline Vs Online Scheduling.

Unit IV: Inter-process Communication
Inter-process Communication and Synchronization of Processes, Tasks and Threads- Multiple Process in an
Application, Problem of Sharing data by multiple tasks & routines, Inter-process communication

Unit V: Real Time Operating Systems & Programming Tools
Operating Systems Services, I/O Subsystems, RT & Embedded Systems OS, Interrupt Routine in RTOS Environment Micro C/OS-II- Need of a well Tested & Debugged RTOs, Use of µCOS-II

Unit VI: VX Works & Case Studies
Memory managements task state transition diagram, pre-emptive priority, Scheduling context switches- semaphore- Binary mutex, counting watch dugs, I/O system

Case Studies of programming with RTOS- Case Study of Automatic Chocolate Vending m/c using µCOS RTOS, case study of sending application Layer byte Streams on a TCP/IP network, Case Study of an Embedded System for a smart card.

TEXT BOOKS:

1. Embedded Systems- Architecture, Programming and Design by Rajkamal, 2nd ed., 2008,TMH.

2. Real Time Systems- Jane W. S. Liu- PHI.

3. Real Time Systems- C.M.Krishna, KANG G. Shin, 1996, TMH

4. Embedded system Design-A unified hardware/ software approach by Frank Vahid, Tony D. Givargis, Johnwiley, 2002.

REFERENCES:

1. Advanced UNIX Programming, Richard Stevens

2. VX Works Programmers Guide

I Year – II Sem.

CMOS ANALOG & MIXED SIGNAL DESIGN

Code: 122DS07

L	T	P	C
4	-	-	3

I. CMOS ANALOG CIRCUITS:

UNIT I
CURRENT SOURCES, SINKS & REFERENCES

The cascode connection, sensitivity and temperature analysis, transient response, layout of simple Current Mirror, matching in MOSFET mirrors, other Current Sources/Sinks.

Voltage dividers, current source self-biasing, band gap voltage references, Beta-Multiplier Referenced Self-biasing.

UNIT II

AMPLIFIERS: Gate Drain connected loads, Current Source Loads, Noise and Distortion, Class AB Amplifier.

FEEDBACK AMPLIFIERS: Feedback Equation, properties of negative feedback and amplifier design, feedback topologies, amplifiers employing the four types of feedback, Stability.

UNIT III
DIFFERENTIAL AMPLIFIERS

The Source Coupled pair, the Source Cross-Coupled pair, cascode loads, Wide-Swing Differential Amplifiers.

UNIT IV
OPERATIONAL AMPLIFIERS

Basic CMOS Op-Amp Design, Operational Transconductance Amplifiers, Differential Output Op-Amp.

II. MIXED SIGNAL CIRCUITS:

UNIT V
NON-LINEAR & DYNAMIC ANALOG CIRCUITS

Basic CMOS Comparator Design, Adaptive Biasing, Analog Multipliers, MOSFET Switch, Switched Capacitor circuits: Switched Capacitor Integrator, dynamic circuits.

UNIT VI
DATA CONVERTER ARCHITECTURES

Data Converter Fundamentals, DAC & ADC specifications, Mixed Signal Layout issues, DAC architectures, ADC architectures.

TEXT BOOKS:

1. CMOS Circuit Design, Layout and Simulation - Baker, Li, Boyce, PHI, 2004.

REFERENCE BOOKS:

1. Analog Integrated Circuit Design - David A. Johns, Ken Martin, 1997, John Wiley & Sons
2. Design of Analog CMOS Circuits – B. Razavi, MGH, 2003, TMH.
3. Analog MOS ICs for Signal Processing – R.Gregorian, Gabor C. Temes, John Wiley & Sons.

I Year – II Sem.

ENTREPRENEURSHIP AND INNOVATION
(OPEN ELECTIVE)

Code: 122MB47

L	T	P	C
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The objective of the course is to make students understand the nature of entrepreneurship, and to motivate the student to start his/her own enterprise with innovative skills.

Unit 1: Nature of Entrepreneurship; Characteristics, Qualities and skills of an Entrepreneur, functions of entrepreneur, Entrepreneur scenario in India and Abroad. Forms of Entrepreneurship: Small Business, Importance in Indian Economy, Types of ownership, sole trading, partnership, Joint Stock Company and other forms. First-Mover disadvantages, Risk Reduction strategies, Market scope strategy, Imitation strategies, and Managing Newness.

Unit 2: Aspects of Promotion: Generation of new entry opportunity, SWOT Analysis, Technological Competitiveness, legal regulatory systems, patents and trademarks, Intellectual Property Rights- Project Planning and Feasibility Studies- Major steps in product development.

Unit 3: MANAGEMENT OF SMALL BUSINESS:

Pre feasibility study - Ownership - budgeting - project profile preparation - Feasibility Report preparation - Evaluation Criteria- Market and channel selection- Product launching - Monitoring and Evaluation of Business- Effective Management of Small business.

Unit 4: SUPPORT SYSTEMS FOR ENTREPRENEURS:
Institutional Support, Training institution, Financial Institutions and Aspects: Sources of raising Capital, Debt-Equity, Financing by Commercial Banks, Government Grants and Subsidies, Entrepreneurship Promotion Schemes of Department of Industries (DIC), KVIC, SIDBI, NABARD, NSIC, APSFC, IFCI and IDBI. New Financial Instruments. Research and Development – Marketing and legal aspects, Taxation benefits, Global aspects of Entrepreneurship.

Unit 5: INTRODUCTION TO INNOVATION:
Meaning of innovation, sources of innovative opportunity, 7 sources of innovative opportunity, Principles of innovation, the enablers of innovation, business insights, insights for innovation, technical architecture for innovation, focus on the essence of innovation.

Unit 6: PROCESS AND STRATEGIES FOR INNOVATION:
Process of innovation, the need for a conceptual approach, Factors contributing to successful technological innovation, Strategies that aim at innovation, impediments to value creation and innovation.

Text Books:

1. Robert D Hisrich, Michael P Peters, Dean A Shepherd: Entrepreneurship, TMH, 2009
2. H. Nandan: Fundamentals of Entrepreneurship, PHI, 2009.

References:

1. Bholanath Dutta: Entrepreneurship – Text and cases, Excel, 2009.
3. Vasanth Desai: Entrepreneurship, HPH, 2009
4. Barringer: Entrepreneurship, Pearson,2009.
5. Peter Drucker (1993), “Innovation and Entrepreneurship”, Hyper Business Book.
6. C.K. Prahalad, M.S. Krishnan, The new age of Innovation – Tata McGraw-Hill,Edition 2008

I Year – II Sem.
NETWORK SECURITY AND CRYPTOGRAPHY
(OPEN ELECTIVE)

Code: 122SE20

L	T	P	C
4	-	-	3

UNIT - I
Security Attacks (Interruption, Interception, Modification and Fabrication), Security Services (Confidentiality, Authentication, Integrity, Non-repudiation, access Control and Availability) and Mechanisms, A model for Internetwork security, Internet Standards and RFCs.

UNIT - II
Conventional Encryption Principles, Conventional encryption algorithms: DES, TDES, AES, cipher block modes of operation, location of encryption devices, key distribution, Approaches of Message Authentication, Secure Hash Functions: SHA1 and HMAC.

Public key cryptography principles, public key cryptography algorithms: RSA, DIFFIE HELL MAN, digital signatures, digital Certificates, Certificate Authority and key management

Kerberos, X.509 Directory Authentication Service.

UNIT - III
Email privacy: Pretty Good Privacy (PGP) and S/MIME.

UNIT - IV
IP Security Overview, IP Security Architecture, Authentication Header, Encapsulating Security Payload, Combining Security Associations and Key Management.

UNIT – V
Web Security Requirements, Secure Socket Layer (SSL) and Transport Layer Security (TLS), Secure Electronic Transaction (SET).
Intruders, Viruses and related threats.

UNIT - VI
Firewall Design principles, Trusted Systems. Intrusion Detection Systems.

TEXT BOOKS :

1. Network Security Essentials (Applications and Standards) by William Stallings Pearson Education.

2. Hack Proofing your network by Ryan Russell, Dan Kaminsky, Rain Forest Puppy, Joe Grand, David Ahmad, Hal Flynn Ido Dubrawsky, Steve W.Manzuik and Ryan Permeh, wiley Dreamtech

REFERENCES:

1. Fundamentals of Network Security by Eric Maiwald (Dreamtech press)

2. Network Security - Private Communication in a Public World by Charlie Kaufman, Radia Perlman and Mike Speciner, Pearson/PHI.

3. Cryptography and network Security, Third edition, Stallings, PHI/Pearson

4. Principles of Information Security, Whitman, Thomson.

5. Network Security: The complete reference, Robert Bragg, Mark Rhodes, TMH

6. Introduction to Cryptography, Buchmann, Springer.

I Year – II Sem.

ADVANCED OPERATING SYSTEM (OPEN ELECTIVE)

Code: 122SE21

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UNIT I

Introduction to Operating Systems: Overview of computer system hardware, Instruction execution, I/O function, Interrupts, memory hierarchy, I/O communication techniques, operating system objectives, and functions and evaluation of operating system.

UNIT II

Introduction to UNIX and LINUX: Basic commands and command arguments, Standard input/output; Input/output re-direction, filters and editors, shells and operations.

UNIT III

System Calls: System calls and related file structures, Input/output, Process creation and termination.

UNIT IV

Inter Process Communication: Introduction, file and record locking, client-server example, pipes, FOFOs, streams &messages, name spaces, Systems V IPC, message queues, semaphores, shared memory, sockets & TLI.

UNIT V

Introduction to Distributed systems: Goals of distributed system, Hardware and Software concepts, Design issues.

Communication in Distributed Systems: Layered protocols, ATM networks, client-server model, Remote procedure call and group communication.

UNIT VI

Synchronization in Distributed systems: Clock synchronization, mutual extension, E-tech algorithms, Bully algorithm, Ring algorithm, Atomic transactions.

Deadlocks: Deadlock in distributed systems, Distribution deadlock prevention and distributed deadlock detection.

TEXT BOOKS

1. The design of the UNIX Operating Systems – Maurice J.Bach, 1986, PHI
2. Distributed Operating System - Andrew S. Tennenbaum, 3rd d. PHI
3. The Complete reference LINUX – Richard Peterson, 4th ed. McGaw Hill

REFERENCES:

1. Operating Systems: Internal and Design Principals, Stallings, 6th ed. PE.
2. Modern Operating Systems, Andrew S. Tennenbaum, 3rd ed. PE
3. Operating System Principles – Abraham Silberchatz, Peter B. Galvin, Gre Gagne, 7th ed. John Wiley.
4. UNIX User Guide – Ritchie & Yates.
5. Unix Network Programming – W. Richard Stevens, 1998 PHI
6. The UNIX Programming Environment – Kernighan & Pike, PE

I Year – II Sem.
RESARCH METHODOLOGY
(OPEN ELECTIVE)

Code: 122SE22

L	T	P	C
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Unit- I :

- What is Research?
- What is not Research?
- Meaning, aim, nature and scope of research
- Characteristics and Prerequisites of research.
- Research needs in Engineering, Education, Science and Management.
- Research benefits to Society in general.

Unit II

- Role of Review.
- Search for related literature.
- On line search.
- Searching Web
- Conducting a literature search.
- Evaluating, Organizing, and synthesizing the literature.

Unit- III

- Identifying and describing the research .
- Finding the research Problem.
- Sources of research problem.
- Criteria/ Characteristics of a Good research.

Unit – IV

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- The Nature and role of Data in Research.
- Linking Data and Research Methodology.
- Validity of Method.
- Planning for Data collection.
- Choosing a Research Approach.
- Use of Quantitative / Qualitative Research Design.
- Feasibility of Research Design.
- Establishing Research Criteria.
- Justification of Research Methodology.

Unit- V

- Characteristics of a proposal.
- Formatting a research proposal.
- Preparation of proposal.
- Importance of Interpretation of data and treatment of data.

Unit- VI

- Format of the Research report.
- Style of writing report.
- References and Bibliography.

REFERENCES

1. Practical Research : planning and Design(8th Edition) – Paul D. Leedy and Jeanne E. Ormrod.
2. www. Prenhall.com/leedy.
3. A Hand Book of Education Research – NCTE
4. Methodogy of Education Research – K.S. Sidhu.
5. Research Methodology. Methods & Technique : Kothari. C.R.
6. Tests, Measurements and Research methods in Behavioural Sciences- A.K. Singh.
7. Statistical Methods- Y.P. Agarwal.
8. Methods of Statistical Ananlysis- P.S Grewal.
9. Fundamentals of Statistics – S.C. Gupta, V.K. Kapoor.

I Year – II Sem.
IMAGE & VIDEO PROCESSING
(ELECTIVE – III)

Code: 122DS05

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UNIT I: Fundamentals of Image Processing and Image Transforms

Basic steps of Image Processing System Sampling and Quantization of an image – Basic relationship between pixels
Image Transforms: 2 D- Discrete Fourier Transform, Discrete Cosine Transform (DCT), Wavelet Transforms: Continuous Wavelet Transform, Discrete Wavelet Transforms.

UNIT II: Image Enhancement

Spatial domain methods: Histogram processing, Fundamentals of Spatial filtering, Smoothing spatial filters, Sharpening spatial filters.
Frequency domain methods: Basics of filtering in frequency domain, image smoothing, image sharpening, Selective filtering.

UNIT III: Image Segmentation & Compression

Image Segmentation concepts, Point, Line and Edge Detection, Thresholding and Region Based segmentation. Image compression fundamentals - Coding Redundancy, Spatial and Temporal redundancy, Compression models: Lossy & Lossless, Huffman coding, Arithmetic coding, LZW coding, Run length coding, Bit plane coding, Transform coding, Predictive coding.

UNIT IV: Basic steps of Video Processing

Analog Video, Digital Video. Time-Varying Image Formation models: Three-Dimensional Motion Models, Geometric Image Formation, Photometric Image Formation, Sampling of Video signals and filtering operations.

UNIT V: 2-D Motion Estimation

Optical flow, General Methodologies, Pixel Based Motion Estimation, Block-Matching Algorithm, Mesh based Motion Estimation, Global Motion Estimation, Region based Motion Estimation, Multi resolution motion estimation, Application of motion estimation in Video coding.

UNIT VI: Three dimensional Motion Estimation & Waveform based coding
Feature based motion estimation, Direct Motion Estimation. Block based transform coding, Predictive Coding.

TEXT BOOKS

1. Digital Image Processing – Gonzaleze and Woods, 3rd ed., Pearson.

2. Video processing and communication – Yao Wang, Joem Ostermann and Ya–quin Zhang. 1st Ed., PH Int.

REFERENCE BOOKS

1. Digital Video Processing – M. Tekalp, Prentice Hall International

I Year – II Sem.
DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES
(ELECTIVE III)

Code: 122DS08

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UNIT I
INTRODUCTION TO DIGITAL SIGNAL PROCESING
Introduction, A Digital signal-processing system, The sampling process, Discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation, Analysis and Design tool for DSP Systems MATLAB, DSP using MATLAB.

UNIT II
COMPUTATIONAL ACCURACY IN DSP IMPLEMENTATIONS
Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT III
ARCHITECTURES FOR PROGRAMMABLE DSP DEVICES
Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External interfacing.

UNIT IV
EXECUTION CONTROL AND PIPELINING
Hardware looping, Interrupts, Stacks, Relative Branch support, Pipelining and Performance, Pipeline Depth, Interlocking, Branching effects, Interrupt effects, Pipeline Programming models.

PROGRAMMABLE DIGITAL SIGNAL PROCESSORS
Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX processors, Pipeline Operation of TMS320C54XX Processors.

UNIT V
IMPLEMENTATIONS OF BASIC DSP ALGORITHMS
The Q-notation, FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, PID Controller, Adaptive Filters, 2-D Signal Processing.

IMPLEMENTATION OF FFT ALGORITHMS
An FFT Algorithm for DFT Computation, A Butterfly Computation, Overflow and scaling, Bit-Reversed index generation, An 8-Point FFT implementation on the TMS320C54XX, Computation of the signal spectrum.

UNIT VI

INTERFACING MEMORY AND I/O PERIPHERALS TO PROGRAMMABLE DSP DEVICES

Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).

A Multichannel buffered serial port (McBSP), McBSP Programming, a CODEC interface circuit, CODEC programming, A CODEC-DSP interface example.

TEXT BOOKS

1. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.

2. DSP Processor Fundamentals, Architectures & Features – Lapsley et al. S. Chand & Co, 2000.

REFERENCES

1. Digital Signal Processors, Architecture, Programming and Applications – B. Venkata Ramani and M. Bhaskar, TMH, 2002.

2. Digital Signal Processing – Jonatham Stein, John Wiley, 2005.

I Year – II Sem. M.Tech.(VLSI & Embedded Systems)
SEMICONDUCTOR MEMORY DESIGN AND TESTING
(ELECTIVE III)

Code: 122VE10

L	T	P	C
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UNIT I:
Random Access Memory Technologies: SRAM - SRAM Cell Structures, MOS SRAM architecture, MOS SRAM cell and peripheral circuit operation, Bipolar SRAM technologies, SOI technology, Advanced SRAM architectures and technologies, Application specific SRAMs ; DRAM – DRAM technology development CMOS DRAM, DRAM cell theory and advanced cell structures, BiCMOS DRAM, soft error failure in DRAM, Advanced DRAM design and architecture, Application specific DRAM.

UNIT II:
Non-Volatile Memories: Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMs, EPROM, floating gate EPROM cell, one time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash memories (EPROM or EEPROM), advanced Flash memory architecture.

UNIT III:
Memory Fault Modeling Testing and Memory Design for Testability & Fault tolerance: RAM fault modeling, electrical testing, pseudo random testing, megabit DRAM testing, non-volatile memory modeling and testing, IDDQ fault modeling and testing, application specific memory testing, RAM fault modeling, BIST techniques for memory.

UNIT IV:
Semiconductor Memory Reliability: General reliability issues, RAM failure modes and mechanism, non-volatile memory reliability, reliability modeling and failure rate prediction, design for reliability, reliability test structures, reliability screening and qualification.

UNIT V:
Semiconductor Memory Radiation Effects: Radiation effects, Single event phenomenon (SEP), radiation hardening techniques and design issues, radiation hardened memory characteristics, radiation hardness assurance and testing, Radiation Dosimetry, Water level radiation testing and test structures.

UNIT VI:
Advanced Memory Technologies and High-Density Memory Packing Technologies: Ferroelectric RAMs (FRAMs), GaAs FRAMs, analog memories, magneto resistive RAMs (MRAMs), experimental memory devices, memory hybrids and MCMs (2D), memory stacks and MCMs (3D), memory MCM testing and reliability issues, memory cards, high density memory packaging future directions.

TEXT BOOKS

1. Semiconductor Memories Technology, Ashok K. Sharma, 2002, Wiley.

2. Advanced Semiconductor Memories – Architecture, Design and Applications; Ashok K. Sharma, 2002, Wiley.

3. Modern Semiconductor Devices for Integrated Circuits, Chenming C. Hu, 1st ed. Prentice Hall.

I Year – II Sem. M.Tech.(VLSI & Embedded Systems)
EMBEDDED SYSTEMS LAB

Code : 122VE73

L	T	P	C
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Research Methodology:

Research Methodology: An Introduction; Defining the Research Problem; Overview of – (i) Research Design, (ii) Sampling Design, (iii) Measurement and Scaling Techniques, (iv) Methods of Data Collection, (v) Processing and Analysis of Data, (vi) Interpretation and Report Writing.

Text Books:

1. Research Methodology: Methods and Techniques, C.R. Kothari, 2nd ed. New Age International.

2. Research in Education, Best & Kahn, 9th ed. 2006, PHI

LIST OF EXPERIMENTS:

CYCLE 1 : 8051 MICROCONTROLLERS

Serial data Transmission using 8051 microcontroller in different modes

Look up tables for 8051

Timing subroutines for 8051 – Real time and applications

Keyboard interface to 8051

ADC, DAC interface to 8051

LCD interface to 8051

CYCLE 2 :

Study of Real Time Operating Systems

Development of Device Drivers for RT Linux

Software Development for DSP Applications

Serial Communication Drivers for ARM Processors

Case Studies : Any Two –

Design of RTOS Kernel

Cross Compiler / Assembler

Vx Works

I Year – II Sem. M.Tech.(VLSI & Embedded Systems)
TECHNICAL SEMINAR (Independent Review Paper)
Code: 122VE74

L	T	P	C
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Max. Marks: 50

There shall be two seminar presentations during I year I semester and I year II Semester. For seminar, a student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the Department in a report form and shall make an oral presentation before the Departmental Committee, which shall consist of the Head of the Department, a senior Faculty Member and the Supervisor and will jointly evaluate the report and presentation. For each Seminar there will be only internal evaluation of 50 marks. A candidate has to secure a minimum of 50% to be declared successful.

In the First semester the report must be in the form of the review paper with a format used by IEEE / ASME etc. In the Second semester Technical Seminar in the form of Independent Review Paper must be of high quality fit for publication in a reputed conference / journal.

The evaluation format for seminar is as follows:

- Day to day evaluation by the Supervisor : 10 marks
- Final Report : 10 marks
- Presentation : 30 marks

II Year – I Sem.
COMPREHENSIVE VIVA-VOCE

Code: 122VE75

L	T	P	C
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Max. Marks: 50

There shall be a Comprehensive Viva-Voce in II year I Semester. The Comprehensive Viva-Voce will be conducted by a Committee consisting of Head of the Department and two Senior Faculty members of the Department. The Comprehensive Viva-Voce is aimed to assess the students' understanding in various subjects he/she studied during the M.Tech course of study. The Comprehensive Viva-Voce is valued for 50 marks by the Committee. There are no internal marks for the Comprehensive Viva-Voce. A candidate has to secure a minimum of 50% to be declared successful.

II Year – I Sem. M.Tech.(VLSI & Embedded Systems)
PROJECT SEMINAR

Code: 122VE76

L	T	P	C
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Max. Marks: 50

In II year I semester, a project seminar shall be conducted for 50 marks and for 2 credits (there is no external evaluation). The evaluation for the project seminar shall be done in two stages, i.e. in the middle of the semester and at the end of the semester. The mid-semester seminar evaluation shall carry 25 marks and the end semester seminar evaluation shall carry 25 marks. The report for the project seminar will carry 10 marks and remaining marks (15M) shall be for presentation and discussion. A candidate shall secure a minimum of 50% to be declared successful.

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II Year – I Sem.
PROJECT WORK (PART I)
PROJECT STATUS REPORT

Code: 122VE77

L	T	P	C
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Every candidate shall be required to submit thesis or dissertation after taking up a topic approved by the Project Review Committee.

A Project Review Committee (PRC) shall be constituted comprising of Heads of all the Departments which are offering the M.Tech programs and three other senior faculty members concerned with the M.Tech. programme.

Registration of Project Work: A candidate is permitted to register for the project work after satisfying the attendance requirement of all the previous semesters and after obtaining the approval of the PRC.

After satisfying 6.2, a candidate has to submit, in consultation with his project supervisor, the title, objective and plan of action of his project work to the PRC for its approval. Only after obtaining the approval of PRC the student can initiate the Project work. This process is to be completed within four weeks of commencement of II year I semester.

The student shall submit a project report at the end of II year I semester, and the same shall be evaluated at the end of that semester by the PRC as Excellent/Good/Satisfactory/Unsatisfactory. In the case of Unsatisfactory declaration, the student shall re-submit the Project report after carrying out the necessary modifications / additions in the Project work, within the specified time as suggested by the PRC.

II Year – II Sem.
PROJECT SEMINAR

Code: 122VE78

L	T	P	C
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Max. Marks: 50

A project seminar shall be conducted for 50 marks and for 2 credits (there is no external evaluation). The evaluation for the project seminar shall be done in two stages, i.e. in the middle of the semester and at the end of the semester. The mid-semester seminar evaluation shall carry 25 marks and the end semester seminar evaluation shall carry 25 marks. The report for the project seminar will carry 10 marks and remaining marks shall be for presentation and discussion. The report for end semester project seminar shall be for 10 marks and the remaining marks(15M) shall be for presentation and discussion. A candidate shall secure a minimum of 50% to be declared successful.

II Year – II Sem.
PROJECT WORK AND DISSERTATION

Code: 122VE79

L	T	P	C
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A candidate is permitted to submit Project Dissertation only after successful completion of PG subjects (theory and practical), seminars, Comprehensive viva-voce, PG Project Part–I, and after the approval of PRC, not earlier than 40 weeks from the date of registration of the project work. For the approval of PRC the candidate shall submit the draft copy of thesis to the Head of the Department and shall make an oral presentation before the PRC. Along with the draft thesis the candidate shall submit draft copy of a paper in standard format fit for publication in Journal / Conference, based on the project thesis, to the Head of the Department with due recommendation of the supervisor.

- Four copies of the Project Dissertation certified by the Supervisor and Head of the Department shall be submitted to the College.

- The dissertation shall be adjudicated by one examiner selected by the College. For this, Head of Department shall submit a panel of 3 examiners, who are eminent in that field, with the help of the PRC. The Chief Superintendent of the college in consultation with the college academic committee shall nominate the examiner.

- If the report of the examiner is not favourable, the candidate shall revise and resubmit the Dissertation, in the time frame as prescribed by PRC. If the report of the examiner is unfavourable again, the thesis shall be summarily rejected. The candidate can re-register only once for conduct of project and evaluation of Dissertation, and will go through the entire process as mentioned above. The total duration for the M.Tech program is limited to four years.

- If the report of the examiner is favourable, viva-voce examination shall be conducted by a Board consisting of the Head of the Department, Supervisor and the Examiner who adjudicated the Dissertation. The Board shall jointly report the student's performance in the project work as – (a) Excellent, or (b) Good, or (c) Satisfactory, or (d) Unsatisfactory, as the case may be. In case, the student fails in the viva-voce examination, or gets the Unsatisfactory grade, he can re-appear only once for the viva-voce examination, as per the recommendations of the Board. If he fails at the second viva-voce examination, the candidate can re-register only once for conduct of project and evaluation of Dissertation, and will go through the entire process as mentioned above. The total duration for the M.Tech program is limited to four years.