Dr. D. Ajitha, MISTE, AMIETE
Associate Professor (ECE)
B.Tech. (Electronics), M.Tech (VLSI System Design), Ph. D. (JNTUA, Anantapur)
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Career Highlights

10^{+}years of academia teaching (U.G and P.G) experience

- **ECE Department, Sreenivasa institute of technology and management studies, Chittooor**
- **Sreenidhi Institute of Science and Technology (SNIST),**Hyderabad, India

Patents Filed and Published

1. ***Patent application # 201941022350A***- Bit Synchronizer for Biphase Input with Variable Bit-Rate: **- Application Year 2019**

Research Interests

VLSI Circuit Design, Nanotechnology (QCA) And
Reversible logic

Courses Taught

Digital Logic Design, Micro Processors and Interfacing, Microprocessors and Microcontrollers, Switching Theory and Logic Design, C.O, Electronic Devices & Circuits, Digital IC Applications, VLSI Design, Electronic Measurements and Instrumentation, Digital design through Verilog, **PG**: Digital IC design, T.T, ASIC design.

Education

Ph.D. - ECE Dept. Digital VLSI circuits, JNTU College of Engineering, Anantapur, 2017.

Doctoral Dissertation – **DESIGN, DEVELOPMENT & PERFORMANCE COMPARISON OF NANO CIRCUIT LIBRARIES FOR VLSI CIRCUITS USING QCA**

M.Tech. - ECE Dept. – VLSI System Design, JNTUA, Anantapur, 2009, First Class with Distinction (78%)

Master Thesis - A Novel On-Line Testable Reversible Adders with New Reversible Gate

B.Tech (Electronics & Communication Engineering), First class with Distinction (71%), JNTU, Hyderabad, 2006.

Final Year Project– A New Approximation Method for CAC Schemes in Cellular Mobile Networks.

Awards

Best Paper award at *SCOReD 2015* Conference, Kuala Lumpur, Malaysia.