Dr. Ramani S

B.E., M.E., Ph.D. LMISTE, IEEE

Associate Professor (ECE)

B.E.(ECE), M.E(Applied Electronics)

Ph.D.(Anna University)

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Key Strengths across Experience

- As **Head of the Department for ECE** more than 6 years (Varuvan Vadivelan Institute of Technology – Dharmapuri)
- Organized various **workshop and conference** and presented papers and seminar sessions. Acted as Coordinator NBA **/ *ISO*** activities
- More than 70 projects for **BE ECE**/EEE students More than 50 project for **PG** (ME-CS, ME-AE, Msc-Electronics, MCA etc...)
- Have 21 years of teaching experience in Engineering Colleges at various capacities.
- Published more than 31 International Conference Papers and referred journals.
- 7 years of extensive experience in Research in the areas of Embedded Networking /Simulation.

Career Highlights

Period		No. of Years	Designation / Nature of job	Institute /Organization
From	To			
03/01/17	Till date	-	Associate Professor	Sreenidhi Inst. of Science & Technology Hyderabad **(JNTU)**
14/02/11	31/12/16	6	Associate Prof / HOD	Varuvan Vadivelan Institute of Technology (**Anna University**)
01/02/07	28/02/11	4	Assistant Professor	Er.Perumal Manimegallai College of Engineering. (**Anna University**)
22/05/05	31/01/07	2	SL & Ast.Prof	The Oxford College of Engineering – Bangalore**(VTU)**
10/6/00	12/06/03	3	Lecturer	Priyadharshini Engg. College **(MU/AU)**
1998	2000	2	P.Time Lecturer	Govt. College of Engineering (Burgur) (**Madras University**)

Education

Ph.D. :- ECE Dept., Anna University. Dec 2017: BE and Slack Time Based NoC for Humanizing the QoS Performance in Inter Domain Networks.

Doctoral Dissertation – *The NoC system has mainly been indirect to the problem posed by the interconnection*

between nodes in the network. Although there is a consensus about using networks inside the chip, the trend has been so far to borrow the methods and solutions from the networking and interconnection networks field without entirely taking into account the "on-chip" context. It is believed that the right approach should start from the on-chip context and adapt the existing findings from the other areas to the specificities of being inside a single chip. This should not be limited to synchronization, power consumption, and wire-routing. Other aspects like overhead, complexity, design-time reduction are also considered. The on-chip context offers more advantages than the inter-chip context. Determinism of communication and locality, all the nodes are local and versatility of available components. The network elements are hardware models that can be parameterize and changed, but in physical components that are fixed and cannot be changed.

M.E.: - ECE Dept. – Applied Electronics. MAY 2005 , Sathyabama University 77%

B.E. :- ECE Dept. Madras University, Chennai. India 1998

Final Year Project– *Test ZiG of Missile,* **B.E.L Chennai, India**